Lab of Computational Microelectronics

2011 Published Papers & Patents
(計算微電子實驗室 Proposal)

By

Gene Sheu

Asia University    Jan 5, 2012
Preface

This section shows the academic paper contributions to microelectronics computational engineering during the recent 2 years in Asia University.

The published papers can be divided by 4 parts:

1) **Analytical Solution** using by computation of computer language, such as Matlab, C language … and so forth.

2) **Computation of Mesh Generation** to obtain high accuracy, more efficiency running time of computer calculation and predictable simulation data as compared to experimental data

3) **Computation of Reliability** such as ESD testing, latch-up immunity, thermal SOA (safe-operation-area)… and so forth in power semiconductor devices

4) **Computation of Process and Device Simulation** to optimize the fabricating process condition and device operating characteristics
一．2011 論文發表與投稿目錄，共發表 20 篇 EI、SCI 等級著名國際論文及專利申請（共 2 篇）


7. Jung-Ruey Tsai, Yuan-Min Lee, Min-Chin Tsai, Gene Sheu, and Shao-Ming Yang, “Development of ESD Robustness Enhancement of a Novel 800V LDMOS


11. Manoj Kumar, Gene Sheu, Jung-Ruey Tsai, Shao-Ming Yang, and Yu-Feng Guo, “A new methodology to investigate the effect of stress and bias on 2DEG and drain current of AlGaN/GaN based heterostructure”, IEEE CSTIC 2012 (accepted, EI).


16. Briliant Adhi Prabowo, Surya Kris Amethystna, Gene Sheu, Jung-Ruey Tsai and Shao-Ming Yang, “Interface Trap Mapping for HCI Reliability Assessment on
Bend Gate Structure”, IEEE 19th International Symposium on the Physical and Failure Analysis of Integrated Circuits, IPFA 2012. (has been submitted, EI)

17. Purwadi, Shu-Ming Bai, Briliant Adhi Prabowo, Jung-Ruey Tsai, Sao Ming Yang and Gene Sheu, “Overlapping Pulse Time-Induced Latch-up Investigation in Bootstrapping Technique”, IEEE 19th International Symposium on the Physical and Failure Analysis of Integrated Circuits, IPFA 2012. (has been submitted, EI)


19. Jung-Ruey Tsai, Jia-Ming Guo, Shao-Ming Yang, Gene Sheu, “A 200V Enhanced Dual Conduction Layer LDMOS with 12um Drift Region,” (to be submitted.)


Application of Multi-Lateral Double Diffused Field Ring in Ultrahigh-Voltage Device MOS Transistor Design

Yang Shaoming, Sheu Gene, Guo Jiaming, Tasi Jung Ruey
Department of Computer Science and Information Engineering, Asia University
500, Lioufeng Rd., Taichung, 41354, China
Email: rickyyang121@asia.edu.tw

Abstract – A novel ultrahigh-voltage device with multi-lateral double diffused field ring in reduced surface field (RESURF) lateral double-diffused MOS (LDMOS) transistor in junction-isolated power IC technology is developed and successfully simulated. The multiple rings of P+ implant used linearly p-top mask design to form multi-lateral diffused field ring to cause many depletion regions. Due to charge balance effect, the multiple p-top rings makes the doping concentration of the N-drift region increased to cause the specific on-resistance reduced. The proposed multiple p-top rings RESURF LDMOS device is able to achieve a specific on-resistance of lower than 144.7 mΩ cm² while maintaining a breakdown voltage of over 800 volts.

Keywords – RESURF, LDMOS, linear p-top rings, on-resistance, charge balance.

I. INTRODUCTION

In recent years, the development of single chip process for integrating power switches with control circuitry is a major trend in the field of power IC development. The lateral diffused metal-oxide semiconductor (LDMOS) process in particular is currently being applied to manufacture monolithic ICs for system-on-chip (SoC). The integrated power devices have found various applications both in industrial and consumer equipments such as mobiles, displays, automotive- electronics and telecommunication circuits. The LDMOS process involves performing planar diffusion on the surface of a semiconductor substrate to form a main current path oriented in the lateral direction. The reduced surface field (RESURF) technology has been widely used to construct lateral high-voltage MOSFETs [1-5].

An RESURF LDMOS process using a reduced surface electric field technique with a low thickness Si-epi or N-well can achieve a high voltage with low on-resistance. In recent developments, many high-voltage LDMOS transistors have been proposed. Although there have been many LDMOS constructed, however the drawback of these devices are having higher on-resistance. Therefore, some researchers have proposed high voltage and low on-resistance LDMOS transistors through various methods and processes. Even though a high voltage and low on resistance LDMOS transistor has been manufactured in some companies, the complexity of the production processes increases the production cost and/or reduces the production yield. Another problem is due to quality control in reliability measurement. Some devices will have problem, even though they yield good performance for other electrical behaviors.

In this paper, we develop multi-lateral double diffused field ring in ultrahigh-voltage LDMOS device to realize a high breakdown voltage, low on resistance, good charge balance sensitivity. Employ the multiple rings of P+ implant with linearly p-top rings mask design [6,7]. From the net charges, the P+ implant multiple rings cause the surface look like linearly N-drift to achieve a specific on-resistance of lower than 144.7 mΩ cm² while maintaining a higher breakdown voltage.

II. DEVICE SIMULATION

The conventional RESURF LDMOS transistors schematic cross-sections simulation which include single RESURF LDMOS and double RESURF with uniform p-top have been realized are shown in Fig. 1(a) and Fig. 1(b). Most of the on-state resistance of single RESURF LDMOS device from the long n-drift region is determined. Therefore, the doping concentration of n-drift region in order to obtained lowest possible on-resistance caused by the breakdown voltage decreased. However, the greatest doping of n-drift is to be optimized, so it is very difficult to achieve a desired high breakdown voltage and low on-resistance. Furthermore, the n-drift region should be fully depleted before the electric field in the device reaches the critical field at which avalanche breakdown occurs to meet RESURF requirement [8-10].

Therefore, a new structure is needed to be responsible for increasing the concentration of n-drift region. An improved RESURF LDMOS device can be achieved in another family of devices where an additional layer of opposite conductivity (p-top layer) is to be included in the n-drift region. The double RESURF LDMOS device with uniform p-top is shown in Fig. 1(b). It is main purpose to increase the best charge balance in the drift region of the structure without reducing breakdown voltage. A Linearly Varying Doped (LVD) p-top layer with improved performance for a double RESURF LDMOS has been utilized and proposed that can improve the influence of interconnection related breakdown better than conventional double RESURF structure recently [11]. This device uses single p-top layer inside n-drift region which has linear doping decreases from source end to the drain end.
This novel multiple RESURF LDMOS device is based on the analysis of the double RESURF LDMOS structure with multiple rings is shown in Fig. 1 (c). It is used the linearly p-top rings realized by boron ion implantation through a designed mask which is a sequence of openings, such that p-top layer can be round shape and have linearly doping profile. It only need to change the p-top mask to do p-top rings mask.

III. RESULTS AND DISCUSSION

When the drain bias increases, the depletion layer of n-drift region widens until it punches through to the P-type rings is shown in Fig. 2 (a). After the depletion layer of the drift region reaches the P-type rings, holes in them will flow into the main junction (P-well/N-drift) under the effect of the electric field. Hence, the multiple p-top rings are no longer neutral and exhibits negative. These generated negative charges introduce additional electric field. In the side of the main junction, the direction of the introduced electric field is reverse with the intrinsic electric field. Hence the peak electric field of the main junction edge is reduced. However, the introduced of each ring the edge of the negative charges will create a new peak electric field. However, the reverse electric field between the mutual benefit of each ring, so that the peak electric field less than the critical electric field of silicon by optimizing the rings width and the spacing between them.

Fig.2 (b) shown the exact location of rings relative to the N-drift region is crucial to its effectiveness in increasing the breakdown voltage. So the P-type multiple rings are placed with respect to the N-drift region for optimal charge-balance and better conductive path. The best starting position of the multiple rings is just below the polysilicon gate field plate. Because such a structure can get the maximum electric field area, so there will be the highest breakdown voltage.

Fig. 3 is shown the surface and N-drift electric field distributions for three different technologies of LDMOS structure. The proposed LDMOS with linear P-top rings has more peaks of surface electric field than those of the double RESURF LDMOS with uniform P-top layer and single RESURF LDMOS without P-top layer. The multiple p-top rings structure has lower peak between N-drift and P-substrate under the drain side. Because more peaks of surface electric field, so there will be the highest breakdown voltage. In order to obtain the desired trade-off between breakdown voltage and the specific on-resistance, n-drift region and p-top rings charges of proposed multiple RESURF LDMOS has been varied into several conditions. It is obvious that for p-top rings structure with any given n-drift dose, the breakdown voltage has a
bell-shaped pattern with a plateau of over 800V in response to p-top rings variations.

Therefore, the on-resistance will be going up when the p-top dose increases as depicted in Fig. 5. Thus, p-top dose should be adjusted properly. In addition to get breakdown voltage about 800V, an n-drift dose of 2.8x10^{12} cm^{-2} of p-top rings LDMOS yields the lowest on-resistance compared to the other n-drift conditions for both uniform p-top and p-top rings structures. It can be understood that high n-drift dose leads to low on-resistance that is desirable for high voltage devices. Due to the better breakdown voltage and lower on-resistance region makes the multiple p-top rings device has provided better window for manufacturing.

The main purpose of this introduced p-top rings structure is to minimize the on-resistance while reaching the desired breakdown voltage about 800V, meanwhile the conventional double RESURF and single RESURF structures are not able to achieve that value. The Id-Vd curves of three devices are shown in Fig. 6. The drain current of the multiple rings LDMOSFET is larger that is important factor for improvement of the safe operate area (SOA) than other devices. However, multiple rings device has large SOA. The p-top rings LDMOS a competitive power device for Ultra High Voltage (UHV) applications with high Figure of Merit (FOM).
The multiple p-top rings RESURF LDMOS simulated successfully using the linear p-top rings method. On the basis of the Poisson equation, an analytical model of p-top derived rings mask with excellent improve the implemented of the proposal LDMOS. The linear p-top rings LDMOS structure demonstrates better performance than the commonly used uniform p-top structure and single RESURF structure on the electronic simulation. The result indicates that the p-top rings LDMOS exhibits a breakdown voltage about 800V and specific on-resistance about 144.7 mΩcm². The p-top rings LDMOS a competitive power device for Ultra High Voltage (UHV) applications with high Figure of Merit (FOM).

REFERENCES


AUTHOR BIOGRAPHY

Yang Shaoming was born in Taiwan, China, in 1975. He received the Ph.D degree from Department of Electronics Engineering and Institute of Electronics of National Chiao Tung University, Taiwan, in 2008. He is currently an Assistant professor of Computer Science and Information Technology (CSIE) Department of Asia University, Taiwan, and is the 3D investigator to the joint research & development of LDMOS with Vanguard International Semiconductor Corporation (VIS), a subsidiary company of Taiwan Semiconductor Manufacturing Company (TSMC).
Application of Multi-lateral Double Diffused Field Ring in Ultrahigh-voltage Device MOS Transistor Design

Shao-Ming Yang1*, Gene Sheu1, Jia-Ming Guo, Jung-Ruey Tasi1
1Department of Computer Science and Information Engineering, Asia University 500, Lioufeng Rd., Wufeng, Taichung, Taiwan, Republic of China
Phone: +886-4-2333456 ext.1784, Fax: +886-4-23305737, *Email: rickyyang121@asia.edu.tw

Abstract – A novel ultrahigh-voltage device with multi-lateral double diffused field ring in reduced surface field (RESURF) lateral double-diffused MOS (LDMOS) transistor in junction-isolated power IC technology is developed and successfully simulated. The multiple rings of P+ implant used linearly p-top mask design to form multi-lateral diffused field ring to cause many depletion regions. Due to charge balance effect, the multiple p-top rings makes the doping concentration of the N-drift region increased to cause the specific on-resistance reduced. The proposed multiple p-top rings RESURF LDMOS device is able to achieve a specific on-resistance of lower than 144.7 mΩ cm² while maintaining a breakdown voltage of over 800 volts.

Keywords – RESURF, LDMOS, linear p-top rings, on-resistance, charge balance.

I. INTRODUCTION

In recent years, the development of single chip process for integrating power switches with control circuitry is a major trend in the field of power IC development. The lateral diffused metal-oxide semiconductor (LDMOS) process in particular is currently being applied to manufacture monolithic ICs for system-on-chip (SoC). The integrated power devices have found various applications both in industrial and consumer equipments such as mobiles, displays, automotive-electronics and telecommunication circuits. The LDMOS process involves performing planar diffusion on the surface of a semiconductor substrate to form a main current path oriented in the lateral direction. The reduced surface field (RESURF) technology has been widely used to construct lateral high-voltage MOSFETs [1-5].

An RESURF LDMOS process using a reduced surface electric field technique with a low thickness Si-epi or N-well can achieve a high voltage with low on-resistance. In recent developments, many high-voltage LDMOS transistors have been proposed. Although there have been many LDMOS constructed, however the drawback of these devices are having higher on-resistance. Therefore, some researchers have proposed high voltage and low on-resistance LDMOS transistors through various methods and processes. Even though a high voltage and low on resistance LDMOS transistor has been manufactured in some companies, the complexity of the production processes increases the production cost and/or reduces the production yield. Another problem is due to quality control in reliability measurement. Some devices will have problem, even though they yield good performance for other electrical behaviors.

In this paper, we develop multi-lateral double diffused field ring in ultrahigh-voltage LDMOS device to realize a high breakdown voltage, low on resistance, good charge balance sensitivity. Employ the multiple rings of P+ implant with linearly p-top rings mask design [6,7]. From the net charges, the P+ implant multiple rings cause the surface look like linearly N-drift to achieve a specific on-resistance of lower than 144.7 mΩ cm² while maintaining a higher breakdown voltage.

II. DEVICE SIMULATION

The conventional RESURF LDMOS transistors schematic cross-sections simulation which include single RESURF LDMOS and double RESURF with uniform p-top have been realized are shown in Fig. 1(a) and Fig. 1(b). Most of the on-state resistance of single RESURF LDMOS device from the long n-drift region is determined. Therefore, the doping concentration of n-drift region in order to obtained lowest possible on-resistance caused by the breakdown voltage decreased. However, the greatest doping of n-drift is to be optimized, so it is very difficult to achieve a desired high breakdown voltage and low on-resistance. Furthermore, the n-drift region should be fully depleted before the electric field in the device reaches the critical field at which avalanche breakdown occurs to meet RESURF requirement [8-10].

Therefore, a new structure is needed to be responsible for increasing the concentration of n-drift region. An improved RESURF LDMOS device can be achieved in another family of devices where an additional layer of opposite conductivity (p-top layer) is to be included in the n-drift region. The double RESURF LDMOS device with uniform p-top is shown in Fig. 1(b). It is main purpose to increase the best charge balance in the drift region of the structure without reducing breakdown voltage. A Linearly Varying Doped (LVD) p-top layer with improved performance for a double RESURF LDMOS has been utilized and proposed that can improve the influence of interconnection related breakdown better than conventional double RESURF structure recently [11]. This device uses single p-top layer inside n-drift region which has linear doping decreases from source end to the drain end.
This novel multiple RESURF LDMOS device is based on the analysis of the double RESURF LDMOS structure with multiple rings is shown in Fig. 1 (c). It is used the linearly p-top rings realized by boron implantation through a designed mask which is a sequence of openings, such that p-top layer can be round shape and have linearly doping profile. It only need to change the p-top mask to do p-top rings mask.

III. RESULTS AND DISCUSSION

When the drain bias increases, the depletion layer of n-drift region widens until it punches through to the P-type rings is shown in Fig. 2 (a). After the depletion layer of the drift region reaches the P-type rings, holes in them will flow into the main junction (P-well/N-drift) under the effect of the electric field. Hence, the multiple p-top rings are no longer neutral and exhibits negative. These generated negative charges introduce additional electric field. In the side of the main junction, the direction of the introduced electric field is reverse with the intrinsic electric field. Hence the peak electric field of the main junction edge is reduced. However, the introduced of each ring the edge of the negative charges will create a new peak electric field. However, the reverse electric field between the mutual benefit of each ring, so that the peak electric field less than the critical electric field of silicon by optimizing the rings width and the spacing between them.

Fig.2 (b) shown the exact location of rings relative to the N-drift region is crucial to its effectiveness in increasing the breakdown voltage. So the P-type multiple rings are placed with respect to the N-drift region for optimal charge-balance and better conductive path. The best starting position of the multiple rings is just below the polysilicon gate field plate. Because such a structure can get the maximum electric field area, so there will be the highest breakdown voltage.

Fig. 1. Schematic cross-section simulation structures of conventional (a) single RESURF LDMOS; (b) double RESURF LDMOS; proposed (c) multiple rings RESURF LDMOS utilizing linear p-top.

Fig. 2. (a) the drain bias increases, the depletion layer of n-drift region widens until it punches through to the P-type rings. (b) A comparison of surface electric field distributions for three different starting p-top position technologies of LDMOS at device breakdown.(10um is under the polysilicon field plate).

Fig. 3 is shown the surface and N-drift electric field distributions for three different technologies of LDMOS structure. The proposed LDMOS with linear P-top rings has more peaks of surface electric field than those of the double RESURF LDMOS with uniform P-top layer and single RESURF LDMOS without P-top layer. The multiple p-top rings structure has lower peak between N-drift and P-substrate under the drain side. Because more peaks of surface electric field, so there will be the highest breakdown voltage. In order to obtain the desired trade-off between breakdown voltage and the specific on-resistance, n-drift region and p-top rings charges of proposed multiple RESURF LDMOS has been
varied into several conditions. It is obvious that for p-top rings structure with any given n-drift dose, the breakdown voltage has a bell-shaped pattern with a plateau of over 800V in response to p-top rings variations.

Fig. 3 The surface and N-drift electric field distributions for three different technologies of LDMOS structure at device breakdown.

Fig. 4 shows the sensitivity of breakdown voltage with p-top dose variations for different n-drift dose conditions, in different structure devices. It has been found from both conventional double RESURF and multiple p-top rings structures that increasing p-top implant dose in same n-drift condition will enhance the breakdown voltage to a certain level due to charge balance effect.

Therefore, the on-resistance will be going up when the p-top dose increases as depicted in Fig. 5. Thus, p-top dose should be adjusted properly. In addition to get breakdown voltage about 800V, an n-drift dose of $2.8 \times 10^{12} \text{ cm}^{-2}$ of p-top rings LDMOS yields the lowest on-resistance compared to the other n-drift conditions for both uniform p-top and p-top rings structures. It can be understood that high n-drift dose leads to low on-resistance that is desirable for high voltage devices.

Fig. 5 Sensitivity of on-resistance with p-top dose variations for different n-drift dose conditions, in different structure devices.

The main purpose of this introduced p-top rings structure is to minimize the on-resistance while reaching the desired breakdown voltage about 800V, meanwhile the conventional double RESURF and single RESURF structures are not able to
achieve that value. The Id-Vd curves of three devices are shown in Fig. 7. The conventional single RESURF structures

![Fig. 7](image)

The conventional single RESURF LDMOS; (b) double RESURF LDMOS; (c) proposed multiple rings RESURF LDMOS utilizing linear p-top.

IV. CONCLUSIONS

The multiple p-top rings RESURF LDMOS simulated successfully using the linear p-top rings method. On the basis of the Poisson equation, an analytical model of p-top derived rings mask with excellent improve the implemented of the proposal LDMOS. The linear p-top rings LDMOS structure demonstrates better performance than the commonly used uniform p-top structure and single RESURF structure on the electronic simulation. The result indicates that the p-top rings LDMOS exhibits a breakdown voltage about 800V and specific on-resistance about 145 mΩcm². The p-top rings LDMOS a competitive power device for Ultra High Voltage (UHV) applications with high Figure of Merit (FOM).

ACKNOWLEDGMENT

The author wishes to thank the IEEE for providing this template and all colleagues who previously provided technical support.

REFERENCES

Effects of SiO₂ passivation on AlGaN/GaN HEMT by self-consistent electro-thermal-mechanical simulation

Abijith Prakash, Raunak Kumar, Briliant Adhi Prabowo, Anumeha, Manoj Kumar, Yang Shaoming, Gene Sheu, Jung-Ruey Tsai
Department of Computer Science and Information Engineering, Asia University 500, Lioufeng Rd., Taichung 41354, China
Email: abhi9891@gmail.com

Abstract—We have carried out systematic experiments based on degradation mechanisms of GaN high electron mobility transistors (HEMT). The electro-thermo-mechanical properties of AlGaN/GaN are simulated for reliability testing under different temperature and bias conditions. The effect of surface passivation on undoped AlGaN/GaN HEMT is investigated using SiO₂. This passivation layer can increase the electron density concentration. We have also performed the electro-thermal simulations to study the effect of passivation on selfheating, elastic energy and mechanical stress. Self heating phenomenon seems to be more uniform in case of passivated device. The SiO₂ passivation layer reduces the elastic energy to about 20% comparison with unpassivated device under the gate edge. The elastic energy near the gate edge is reduced which is the critical region for defect formation.

Keywords—High electron mobility transistors, passivation, electro-thermo-mechanical, SiO₂.

I. INTRODUCTION

AlGaN-GaN heterostructure systems are considered to be an important application for microwave application [1-2]. The group III nitrides are strong contenders in the areas of high frequency and high power application due to their wide band gap, hence high breakdown field [3-4]. In spite of this great interest, device reliability is still an important challenge for the wide deployment of AlGaN/GaN HEMT technology. Hence a complete understanding of the reliability of this device is important.

The current collapse is one of the limiting factors which affects the output characteristics of GaN based FET’s [5]. Passivation is one of the methods to reduce the current degradation mechanism. Due to the piezoelectric properties of AlGaN and GaN an inverse piezoelectric effect is generated when voltage is applied and the coupling between electric field and mechanical characteristics give rise to changes in the stress/strain field and thus electronic properties of HEMT [6].

We have discussed the mechanism of SiO₂ surface passivation effects on electrical, thermal and mechanical characteristics of AlGaN/GaN HEMT and compared with unpassivated HEMT. The increase of drain current due to surface passivation by SiO₂ can be attributed due to change in 2DEG concentration. The thermal distribution is seen to be more uniform when the device is passivated. Finally, the stress and elastic energy is estimated from the simulated electric field and temperature profiles obtained from sentaurus simulator. The mechanical stress is total of the intrinsic stress and thermal stress at its respective temperature.

II. SIMULATION PROCESS

The device structure considered in this study is shown in Fig.1. It consists of 2μm undoped GaN layer and 17nm undoped Al₄₀Ga₅₀₋₇₄N barrier layer grown on Silicon substrate. The silicon substrate is doped to a level of 1e20/cm³. The gate contact is 0.65μm wide and the source drain spacing is 5μm. A 400nm thick SiO₂ passivation layer is used for passivation. The above specification is included for the surface unpassivated and passivated device structure. We have coupled the electro-thermal simulations for obtaining the results at different temperature and bias conditions to study the reliability.

![Fig.1 Cross sectional view of undoped AlGaN/GaN structure with 400nm thick SiO₂ passivation layer.](image)

III. RESULTS AND DISCUSSION

A. I-V measurement

Fig.2. shows measured output characteristics of AlGaN/GaN HEMT before and after passivation. The drain currents of SiO₂ passivated devices increased because of 2DEG charge is increased [7]. This is due to the passivation layer that prevents electron injection into the surface trap and hence increases the 2DEG channel concentration. This increases the electron density of the passivated device at the interface as shown in Fig.3. Because the use of SiO₂ passivation layer we can restore the lost current (current collapse). And the increased drain current directly influences the output power.
B. Thermal Distribution

The effect of surface passivation is responsible for uniform temperature distribution. As shown in Fig. 4(a) the passivated device shows uniform distribution of temperature along the device at Vg=0V and Vds=30V. Fig. 4(b) shows the distribution profile of the unpassivated device for same conditions as mentioned in the former case. It clearly shows that passivation affects temperature distribution and SiO2 is a good for uniform temperature distribution. A graphical representation of temperature profiles of unpassivated and passivated device is shown in Fig.4(c).

C. Mechanical stress and Elastic Energy

The elastic energy and mechanical stress of GaN HEMT device increases with high vertical field thereby enhancing the degradation mechanism [8]. We simulate the electric and temperature profiles using Sentaurus simulator. The temperature profiles and their respective electric fields are extracted to calculate the mechanical stress and elastic energy.

\[
\sigma = \sigma_i + \sigma_{th}
\]  

\[
\sigma_i = C_{11}S_1 + C_{12}S_2 + C_{13}S_3 - e_{31}E_z
\]

Where \( \sigma_i \) is intrinsic stress and \( \sigma_{th} \) is thermal stress. The intrinsic stress is calculated from [11]

\[
C_{11} = 29x + 367 \text{ GPa}
\]

\[
C_{12} = 2x + 135 \text{ GPa}
\]

\[
C_{13} = 5x + 103 \text{ GPa}
\]

\[
e_{31} = (-0.11x - 0.49) \times 10^{-4} \text{ C/cm}^2
\]

\[x = \text{Aluminum mole fraction}=0.26\]

The thermal stress is given by

\[
\sigma_{th} = \frac{E_2}{(1-\nu_2)}(\alpha_1 - \alpha_2)(T - T_0)
\]

Where,

\( E_2 \) = Young’s modulus (GPa)

\( \nu_2 \) = Poisson’s ratio

\( \alpha_1 = \) thermal expansion coefficient of GaN/(K)

\( \alpha_2 = \) thermal expansion coefficient of AlGaN/(K)

\( T_0 = \) growth temperature (K) and \( T = \) temperature (K).
The elastic energy per unit area is computed as a function of intrinsic stress given by

\[
W = \frac{1}{C_{11} + C_{12} - \frac{2C_{13}^2}{C_{33}}} \sigma_i^2
\]  

(9)

Where \( \sigma_i \) is the intrinsic stress obtained from equation (2) which is dependent on vertical electric field and \( C_{11}, C_{12}, C_{13} \) and \( C_{33} \) are elastic stiffness constants given by equations (3), (4), (5), and (6). The electric field and temperature profiles are obtained from Sentaurus simulator. These profiles are used for calculation of mechanical stress and elastic energy. The mechanical stress is obtained from equation (1).

Fig 5(a) and 5(b) show the variation of mechanical stress and elastic energy. The device is tested under different uniform lattice temperature conditions. Lattice temperature has impact on the mechanical characteristics of the device. It clearly shows that both mechanical stress and elastic energy decrease with increasing lattice temperature. This data can act as a fingerprint of the device for determining the stress for different temperature conditions and their corresponding electric fields.

In order to perform the passivation effect on mechanical properties of our proposed AlGaN/GaN device we compare the elastic energy of the two. The effect of lattice heating is also shown. Fig. 6 (a) and 6 (b) show the elastic energy distribution for unpassivated and passivated device. The elastic energy at the gate edge seemed to decrease when the operating temperature reached to its typical value of 442K for both cases as shown. We conclude that the elastic energy for passivated device decreases by 20% under the gate edge. Lattice heating and passivation thereby help in reducing the elastic energy at the gate edge which is the critical region for defect formation.

IV. CONCLUSION

The electrical, thermal and mechanical characteristics were discussed before and after passivation. SiO2 proves to suppress the 2DEG depletion and hence prevent the degradation of drain current. A fully coupled electro-thermal simulation and mechanical analysis was carried to study the interrelationship between them. Lattice temperature and its effect on mechanical characteristics were discussed. SiO2 passivation reduces the elastic energy to about 20% under the gate edge in comparison to unpassivated device.

Fig.5 (a) Relationship between mechanical stress, vertical field and lattice temperature of Al0.26Ga0.74N layer in SiO2 passivated GaN HEMTs. (b) Relationship between Elastic energy, vertical field and lattice temperature of Al0.26Ga0.74N layer in SiO2 passivated GaN HEMTs.

Fig.6 (a) Elastic energy of AlGaN/GaN unpassivated HEMT with and without lattice heating condition at Vg=0V and Vd=30V. (b) Elastic energy of AlGaN/GaN passivated HEMT with and without lattice heating condition at Vg=0V and Vd=30V.

REFERENCES


AUTHOR BIOGRAPHY

Abijith Prakash received B.E degree in Telecommunication from BMS Institute of technology, Bangalore, India in the year 2010. He is currently working as a research assistant at Asia University, Taiwan, China, in department of computational microelectronics and pursuing his M.S degree in the same. His research interests include in the areas of reliability testing and high voltage applications of semiconductors. His previous projects dealt with high voltage PNP BJT reliability testing. His current project includes AlGaN/GaN HEMT device simulation and its reliability study. As Gallium nitride approaches high breakdown voltage (about 1650 volts), it’s becoming an important application. So its reliability study becomes important.
Improvement of Electrical Characteristics in LDMOS by the Insertion of PBL and Gate Extended Field Plate Technologies

Min-Chin Tsai, Gene Sheu, Jung-Ruey Tsai* and Shao-Ming Yang

Department of Computer Science and Information Engineering, Asia University
500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China
*Email: jrtsai@asia.edu.tw

Abstract – This article provides a method to improve significantly both of the breakdown voltage and specific on-resistance in high resistivity drift region LDMOS using both of the PBL doping under the source terminal and the gate extended filed plate technologies. The insertion of PBL aims at the reduction of bulk current caused by the impact-ionization-generated holes while the gate extended field plate were be used to shift the impact ionization region from N-drift region surface near the gate side down toward the junction between the P-body and N-drift region to increase the breakdown voltage due to the increase of maximum depletion in the N-drift region.

Keywords – impact ionization, breakdown voltage, on-resistance, LDMOS, field plate, TCAD simulation.

I. INTRODUCTION

Nowadays the lateral double-diffused MOS (LDMOS) has been considered as the conventional power device used in smart power integrated circuits (SPICs) and high voltage integrated circuits (HVICs) applications. High current and high voltage capability are necessarily requested by LDMOS based on the consideration of the safe-operating-area (SOA) in SPICs and HVICs [1, 2]. However, during the high voltage and high current operating, the degradation of device electrical performance and SOA reliability are usually caused by the impact-ionization generated holes phenomenon. As the on-resistance of high voltage device is increased, the power consumption will be also increased due to the high bulk current through the strong impact ionization effect. Therefore, development of device fabricating methods to decrease the bulk current by reducing the impact-ionization generated holes, decreasing the on-resistance and increasing the device breakdown voltage is of great important in high voltage power device application even though the optimization tradeoff is usually between the breakdown voltage, on-resistance and SOA [3].

Hower et. al. [4] had been suggested that the effective base-emitter resistance of the parasitic npn can be reduced by adding the buried body layer with high doping under the source to suppress the turn on of bipolar transistor and improve the electric SOA of LDMOS due to the reduction of drain current. However, the evolution of bulk current due to the decrease of base-emitter resistance of the parasitic npn is not well understood. In addition, it had been proposed that the breakdown voltage and on-resistance of LDMOS can be improved by extended metal field plates from gate electrode due to the modulation of surface potential of the N-drift region [5, 6]. Based on the above mentioned issues, to our best knowledge, this work firstly combined the device fabricating methods of the p+ buried layer (PBL) insertion under the source and gate extended field plate to improve the device electrical performance by reducing the impact-ionization generated holes and shifting the maximum electric field from N-drift surface down toward the junction between the P-body and N-drift region.

II. DEVICE STRUCTURES AND CHARACTERIZATION

A. Design of Device Structure

Figure 1 shows the schematic of a cross-sectional LDMOS with high resistivity n-type drift region and with or without P+ buried layer (PBL) under the N+ source and P+ bulk regions. The high resistivity N-drift region doping was designed to be a conventional doping level of 1×10^{16} \text{ cm}^{-3}, while the doping of the PBL was selected to be a range from 1×10^{18} \text{ cm}^{-3} to 1×10^{20} \text{ cm}^{-3} to investigate its impact on device electrical performance such as the impact-ionization-generated hole effect, breakdown voltage and specific on-resistance. In order to optimal the device breakdown voltage, method of gate extension over the field oxide was also applied instead of the decrease of N-drift region doping method in maintaining the specific on-resistance as low as possible. In addition, the 40 nm gate oxide thickness and a channel length of 0.7 μm were used in the device. P-body doping was selected to be 1×10^{17} \text{ cm}^{-3} while Doping in the drain, source and bulk regions were designed to be a high concentration of 1×10^{20} \text{ cm}^{-3} to perform the optimal ohmic contact and reduce contact resistances.

Figure 2 compares the electric field distributions in the devices with or without the PBL doping ranging from 1×10^{18} \text{ cm}^{-3} to 1×10^{20} \text{ cm}^{-3}. It clear shows that there are two peak of electric field were occurred at the drain side and the junction between the P-body and N-drift region under the gate for the device without PBL operated at on-state. However, the peak of electric field near the drain was much higher than that at the junction. By applying the PBL doping under the P-body region, the maximum electric field near the drain can be reduced and another peak of electric field at the junction can be increased to perform more uniform electric field distribution within the...
N-drift region. The variation of electric field will be saturated with the increase of PBL doping. Figure 3 shows the electric potential distributions in devices with or without PBL. Compared to Fig. 3 (a), it is obvious clearly that the current flow can be confined toward the silicon surface in the P-body region for devices with PBL doping ranging from $1 \times 10^{18}$ to $1 \times 10^{20}$ cm$^{-3}$, as shown in Fig. 3 (b) to Fig.3 (d). Furthermore, it demonstrated that the depletion region will be extended from the P-body/N-drift junction to the channel in the P-body region in devices with PBL, as compared that without PBL. As a result, current path will be confined in the channel and the current flow into the bulk can be reduced with the increase of the PBL doping, as shown in Fig. 3.

It’s well known that the breakdown voltage can be increased with the decrease of N-drift region doping. However, the expansion effect of plateau of drain current cannot be easily suppressed by decreasing the N-drift region doping while maintaining the high breakdown voltage [2, 7]. Figure 4 shows the $I_{ds}$-$V_{gs}$ and $I_{ds}$-$V_{ds}$ characteristics simulated by 2D-device simulator for devices with or with PBL doping effect at the gate voltage of 10 V. It clearly appeared that drain current rises due to the lateral parasitic npn was turn on through the impact-ionization generated hole current as the device worked at drain voltage of about 28 V. The generated holes within the drift and channel regions have strong impact on the distribution of electric potential within the LDMOS to result in the increase of drain and source currents. By adding PBL under the source terminal, however, the expansion effect of drain current can be suppressed to increase the operation region for power LDMOS and the bulk current can be significantly reduced with the increase of the doping of PBL to be about over 30% reduction of that in the device without PBL because the PBL doping can be reduce the base-emitter resistance of the parasitic npn [4].

Figure 5 shows the characteristics of bulk current versus gate voltage at device with or without PBL under drain voltage of 30 V by 2D-device simulation. Conventional bell-shaped characteristics happened at gate voltage lower than 4.2 V while the bulk current increased exponential at high gate voltage bias condition for device with or without PBL. In addition, the second peak of bulk current is higher than the first one is considered reasonably by the Kirk effect induced the high drain current through the impact-ionization generated hole current [7, 8]. The bulk current can be efficiently decreased by adding the PBL under the device source terminal. In addition, the significant power device performances such as the specific on-resistance and breakdown voltage will not degraded due to the insertion of PBL under the source terminal, as shown in Fig. 6. However, the breakdown voltage is still lower than 40 V under the electrical safe-operating-area (SOA) consideration. It had been proposed that the gate extension field plate on the field oxide not only can decrease the specific on-resistance, but also improve the device breakdown whether the metal field plate separated from gate electrode or not. As a result, this work utilized the simple technology of gate plate extension on the field oxide toward the drain side in the device with PBL doping of $1 \times 10^{19}$ cm$^{-3}$ to investigate the device characteristics, as shown in Fig. 7. It observed that the specific on-resistance was significantly decreased with the extended length of gate field plate because the current conductivity can be improved by the increased carrier density in drift region induced by the extended length of high field plate voltage, as shown in Fig. 8. In addition, Fig. 7 also appeared that the breakdown voltage was increased with the extended length of gate field plate. Figure 9 shows the impact ionization regions for device with different gate extended lengths. It suggested that the maximum electric field was shift from N-drift surface near the extended gate plate edge toward the junction between the P-body and N-drift region as the gate extended length was higher than 0.25 μm. Once the impact ionization region goes down to the bulk, the depletion region of N-drift will become larger which will lead the increase of the maximum breakdown voltage. The optimal specific on-resistance and breakdown voltage in this work can be improved by more than 20 % and 19%, respectively, as compared with the device without the PBL and gate extended plate conditions. In addition, we have demonstrated that the substrate hole current will not be increased to maintain the efficient power dissipation of LDMOS due to the extended gate field plate on the field oxide.

**IV. CONCLUSIONS**

This work combined the insertion of PBL under the source terminal and gate extended field plate technologies into LDMOS to improve significantly the device operation performance. The bulk current can be efficiently reduced by the insertion of PBL, which is used to increase the depletion layer under the device channel. By this way, the drain current flow can be confined in the silicon surface and the bulk current can be reduced due to the reduction of base-emitter resistance of the parasitic npn. In addition, the technology of gate extended field plate was used to shift the impact ionization region from N-drift region surface near the gate side down toward the junction between the P-body and N-drift region. By this way, the breakdown voltage can be increased due to the increase of maximum depletion in the N-drift region while maintains the low bulk current.

**ACKNOWLEDGMENT**

We are grateful to the National Center, Taiwan in supporting the High-performance Computing for computer time and facilities.

**REFERENCES**


Fig. 1. Schematics of

Fig. 2. Schematics of

Fig. 3. Schematics of


Fig. 4. Schematics of

Fig. 5. Schematics of

Fig. 6. Schematics of

Fig. 7. Schematics of

Fig. 8. Schematics of
Fig. 9. Schematics of
Analysis of Si3N4 passivation effect by self-consistent electro-thermal-mechanical simulation in AlGaN/GaN heterostructure HEMTs

Raunak Kumar¹ Abijith Prakash¹ Brilian Adhi Prabowo¹ Anumeha¹ Tsai Jung Ruey¹, Gene Sheu¹, Yang Shaoming¹ Guo Yufeng ²
1. Department of Computer Science and Information Engineering, Asia University500, Lioufeng Rd., Taichung, 41354, China
2. School of Electronic Science and Engineering, Nanjing University of Posts and Telecommunications Nanjing, 210096, China
E-mail:jrtai0126@gmail.com

Abstract: The effect of surface passivation on AlGaN/GaN higher electron mobility transistors (HEMT) has been investigated with electro-thermal-mechanical coupling. Electrical, mechanical and thermal properties of AlGaN/GaN HEMTs before and after passivation are analyzed. The drain current increases after passivation because surface passivation reduces the surface state density. Also, planar stress and elastic energy were decreased, as compare the devices with passivation and without passivation conditions. Also, the effect of different lattice heating (uniform heating, no lattice heating) has been studied in this experiment. This shows that the elastic energy in device with uniform heating is lower than that without lattice heating. In this investigation we found that uniform heating will provide elastic energy lower than critical value and with the use of Si3N4, the temperature distribution is very uniform which in turn reduces the stress in AlGaN/GaN HEMTs.

Key Words: high electron mobility transistors, passivation, Si3N4

I. INTRODUCTION

The AlGaN/GaN high electron mobility transistors can be used in many areas like communications, automobile and power devices due to their large band gap, high breakdown electric field and high two-dimensional electron gas (2DEG) concentration [1-2]. The main problem associated with GaN based HEMTs has been how to control the surface trapping effects and improve the device reliability. Ha et al [3], had been proved that AlGaN/GaN HEMTs with passivation suppressed the negative virtual gate effect and current collapse. In spite of this great interest, device reliability is still an important challenge for the wide deployment of AlGaN/GaN HEMT technology. It’s well known that electrical properties and stress can be affected by including electric field and mechanical characteristics because AlGaN and GaN are piezoelectric material [4]. Silicon nitride reduces the surface traps and provides more positive charge at 2DEG layer that removes depletion of 2DEG [5-6]. Due to the inverse piezoelectric effect, mechanical stress can be induced by vertical electric field [7].

In this paper, we have investigated the mechanism of Si3N4 surface passivation on AlGaN/GaN HEMT and compared with unpassivated HEMT simulated by self-consistent electro-thermal-mechanical analysis. Our main concern is AlGaN barrier layer since this region is under high electric field and mechanical stress. In our experiment the drain current is increased by 8% to 20%. Elastic energy decrease by 10% to 13% in comparison between different lattice heating condition (no lattice and uniform lattice heating). In addition, the planar stress and elastic energy also decreases with lattice temperature.

II.DEVICE OVERVIEW

Device reported in this work (as shown in Fig. 1) is based on AlGaN/GaN heterostructure grown on doped (1E16/cm²) Si substrates. The material structure consisted of 17nm undoped Al0.26Ga0.74N barrier and 2μm undoped GaN. Device discussed in this paper have source-drain spacing of 5μm and gate length of 0.65μm. The above specification are included for the unpassivation and compared with 400 nm Si3N4 passivation layer are deposited on source-drain spacing to reduce the current collapse. Source and drain are ohmic contact and gate is schottky contact with schottky barrier 1.5eV.

III.RESULT AND DISCUSSION

This simulation obtained with the use of Synopsys Sentaurus Device simulator and coupled with piezoelectric stress and strain model. The planar stress and elastic energy are calculated for different lattice temperature. Also, different physical lattice heating models selected for simulation. Fig. 2 shows typical DC
output characteristics of AlGaN/GaN HEMT before and after passivation. Gate voltage ($V_g$) is fixed at +1V, 0 V and -1 V and drain voltage ($V_d$) sweep from 0 to 50 V. The improvement of current can be seen in Fig. 2. The improvement of current is recorded up to 8% to 20%. This is due to the passivation layer the electron injection into the surface trap states decreases and so increases the sheet charge density. These increases of the sheet carrier concentration in 2DEG cause the improvement of current with passivation. Because the use of $\text{Si}_3\text{N}_4$ passivation layer we can restore the lost current (current collapse). And the increased drain current directly influences the output power. We can see the total current at 2DEG before and after passivation in Fig. 3 (a) and (b). After passivation the current density at 2DEG region is higher than without passivation. This higher current density indicates the formation of positive charged particles at 2DEG region. The effect of AlN compared to $\text{Si}_3\text{N}_4$ passivation is different in the formation of 2DEG concentration on AlGaN barrier layer. $\text{Si}_3\text{N}_4$ causes tensile stress while AlN induced additional compressive stress, which results in better carrier concentration and mobility in AlN passivation compare to $\text{Si}_3\text{N}_4$ passivation\(^9\).

![Fig. 2 Id vs. Vd sweep from 0 to 50 V for HEMT before and after passivation.](image)

Figure 4 shows the elastic energy profile along the AlGaN channel before and after passivation respectively. In these result it shown that elastic energy decreases after $\text{Si}_3\text{N}_4$ passivation. Elastic energy is directly proportional to electric field so, electric field reduction makes elastic energy lower with passivation. The electric field in AlGaN barrier layer starts from 2DEG region. Electric field and elastic energy are higher at gate edge so, this results in the formation of cracks at the gate edge. Lower in elastic energy at gate edge makes device more reliable with passivation.

![Fig. 3 Total current density formation at 2DEG for HEMT before (a) passivation and (b) after passivation.](image)

![Fig. 4 Elastic energy of the AlGaN layer along the channel for HEMT before passivation and after passivation.](image)

The planar stress and the elastic energy of GaN HEMT increase as the vertical electric field increases, severely degrading device reliability\(^{[3-4]}\). The Planar stress in the presence of electric field in z direction can be written as\(^{[7]}\)

$$\sigma_i = C_{11}S_1 + C_{12}S_2 + C_{13}S_3 - \varepsilon_{31}E_3$$  \hspace{1cm} (1)

Where $\sigma_i$ is intrinsic stress. $C_{11}$, $C_{12}$ and $C_{13}$ are stiffness coefficient. $S_1$ and $S_2$ are planar strain. Both planar strains have same value and it is given by the lattice mismatch between AlGaN and GaN layer. $S_3$ is vertical strain. $E_3$ is vertical component of the electric field along the z direction. $\varepsilon_{31}$ is piezoelectric coefficient. The stiffness coefficient and piezoelectric coefficient depends on mole fraction of Al and it is given by the formula\(^{[9-10]}\)

$$C_{11}(x) = 29x + 367 \text{ GPa}$$  \hspace{1cm} (2)

$$C_{12}(x) = 2x + 135 \text{ GPa}$$  \hspace{1cm} (3)

$$C_{13}(x) = 5x + 103 \text{ GPa}$$  \hspace{1cm} (4)

$$\varepsilon_{31}(x) = -0.11x - 0.49 \text{ C/m}^2$$  \hspace{1cm} (5)

Where,

$x$= mole fraction of Al (0.26)

Stress is also temperature depended. So the total measured stress at an arbitrary temperature is given by\(^{[11]}\)

$$\sigma = \sigma_i + \sigma_{th}$$  \hspace{1cm} (6)

Where,

$\sigma_i$ = Intrinsic stress and

$\sigma_{th}$=Thermal stress

Also,

$$\sigma_{th} = \frac{Ez(\alpha_1 - \alpha_2)(T - T_0)}{(1 - \nu^2)}$$  \hspace{1cm} (7)

Where,
E₂ = Young’s modulus
v₂ = Poisson’s ratio
α₁ = Thermal coefficient of expansion (GaN layer)
α₂ = Thermal coefficient of expansion (AlGaN layer)
T₀ = Growth Temperature

As we discussed in the above equation temperature also affect the induced stress in AlGaN layer. We know that elastic energy is directly proportional to sum of the planar stress and square of vertical electric field so, elastic energy is calculated. Fig. 5 shows the relationship between Elastic energy, electric field and lattice temperature. As show in the Fig. 5, the elastic energy decreases when lattice temperature increases. With increases the lattice temperature Si₃N₄ passivation layer provided more uniform thermal distribution due to which the induced stress and in turn elastic energy also reduced. Also, the passivation will lower down the electric field which reduced elastic energy. Figure 6 shows the relationship between planar stress, electric field and lattice temperature. As show in the Fig. 6 the planar stress decreases when lattice temperature increases. The mechanical stress is induced by electric field under the inverse piezoelectric effect. Equation (6) gives the total stress induced in the AlGaN layer. This planar stress reduced with electric field. At higher lattice temperature the elastic energy and planar stress induced by electric field is lower.

With Si₃N₄ passivation GaN HEMT show the uniform thermal distribution. The uniform thermal distribution is shown in Fig. 7 for the non uniform lattice heating at 442K. The hot spot appear at gate edge and more uniform thermal distribution than unpassivated device.

Figure 8 (a) shows the elastic energy profile along the AlGaN channel of GaN HEMT with no lattice heating and uniform heating condition under ON state (Vg=0V, Vd=50V). As, shown in the Fig. 8 (a) elastic energy is lower by 10% under uniform heating condition compare with no lattice heating, that means lattice heating (with and without lattice) plays a significant role on the mechanical properties of GaN HEMT. Gao et al. [12] demonstrated that uniform lattice heating decreases the elastic energy in AlGaN layer. Also, off state (Vg=-5V, Vd=50V) is demonstrate in Fig. 8 (b) for no lattice and uniform heating. In these result also elastic energy decreases by 12% in uniform heating compare with no lattice heating.
IV. CONCLUSION

We have demonstrated that surface passivation affects the performance of AlGaN/GaN HEMT by depositing Si3N4 which results in the reduction of surface trap effects. The total current density at 2DEG region is higher with passivation indicates reduction of surface traps. This in turn results in the increase of drain current by 8% to 20% when compared to unpassivated device. In this paper we also explained that the elastic energy and electric filed decreases with uniform lattice heating and make device reliable. And planar stress and elastic energy also decreases as the lattice temperature increases.

REFERENCES


AUTHOR BIOGRAPHY

Jung-Ruey Tsai was born in Taiwan, China, 1973. He received the B.S. degree from Feng Chia University, Taiwan, China, in 1998. He then obtained his M.S. degree (2001) and Ph. D degree (2008) from Chang Gung University, Taiwan, China. He had been a post doctor for over 2 years, worked in the department of electronic engineering in Chang Gung University, Taiwan, China, and the department of computer science and information engineering in Asia University, Taiwan China. Now, he is an assistant professor, working at the department of photonics and communication engineering and computer science and information engineering in Asia University, Taiwan. His research interests include dopant activation/deactivation, segregation and diffusion mechanisms in ultra shallow junction devices, the development of transparent thin film transistors and the application of high-k dielectric materials. In addition, he is currently researching on the studying of analog power devices characteristics and reliability.
Self-Consistent Electro-Thermo-Mechanical Analysis of AlN Passivation Effect on AlGaN/GaN HEMTs

Briliant Adhi Prabowo1*, Anumeha1, Abijith Prakash1, Raunak Kumar1, Gene Sheu1,2, Jung-Ruey Tsai1,2**, and Shao-Ming Yang1,

1Department of Computer Science and Information Engineering, Asia University,
2Department of Photonics and Communication Engineering, Asia University
500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China
Email: brilliano@gmail.com * ; jrtsai@asia.edu.tw **

Abstract— In this article, the effect of AlN materials as passivation over AlGaN layer on AlGaN/GaN HEMTs performance was investigated firstly using electro-thermo-mechanical coupled methodology by both TCAD simulation and analytic calculation. It suggested that AlN passivation layer over AlGaN layer effectively spread the surface heat from the channel resulting in reduction of the lattice temperature and enhances the mechanical properties. The drain current in the AlN-passivated device significantly increases about 30% higher than that in unpassivated AlN layer device which is consistent with previous experimental data and demonstrates that the current collapse can be suppressed by dielectric AlN passivation process.

Keywords-AlGaN/GaN, HEMT, AlN passivation, reliability, electro-thermo-mechanical

I. INTRODUCTION

High voltage handling capability of AlGaN/GaN HEMTs has been acknowledged to have a great employment for high power, high temperature and RF device applications. However, the main obstacle in employment of this device is due to its limited electrical reliability. The established device systems could not elucidate reliability issue due to high voltage operation on the device. AlGaN and GaN being piezoelectric materials correlates high voltage to high mechanical stress. The tensile stress in the AlGaN layer increases as a result of electric field induced by high voltage application which also increases the stored elastic energy density in the AlGaN layer. The crystallographic defects formed due to a certain critical elastic energy degrade the electrical characteristics of the device [1]. In addition, the mechanical properties of HEMTs can be significantly influenced by the thermal heating to affect the device operation. It clearly suggests that the thermal heating coupled with inverse piezoelectric effect is induced by the electric field is becoming an important issue on device reliability [2]. Among the various critical issues, the current collapse is very important because microwave output power is limited by this current collapse. The various studies suggest surface states to be responsible for the current collapse. That is, electrons injected from the gate are captured at the surface, which causes decrease in the drain current [3]. It is also reported that suppression of current collapse should be accountable for the reduction of surface traps due to the surface passivation of AlGaN [4]. In addition placing heat-conductive passivation is expected to effectively spread the heat from the channel resulting in reduction of the thermal resistance since the increase in the channel temperature limits the achievable RF output power. Thus, the ideal passivation film is needed to have high thermal conductivity [5]. However, the electro-thermal-mechanical coupling mechanisms of AlN passivated AlGaN/GaN HEMTs is not well understood. In this study, the methodology of combining the electro-thermo TCAD simulation with electro-mechanical analytic calculation was developed to firstly illustrate the AlN-passivated layer effect on AlGaN/GaN HEMTs electrical performance.

II. METHODOLOGY

Electro-thermal model analysis for HEMT AlGaN/GaN device consists of two parts. First, was using drift diffusion transport model to determine vertical electrical field distribution on active layer, and second was using thermodynamic model to obtain lattice temperature profile at the same layer [2,6]. Lattice temperature and vertical electrical field distribution was simulated by using Synopsys Sentaurus Device simulator, while planar stress and elastic energy were calculated. [1,2,7]. Using this methodology, the effect of AlN passivation on AlGaN/GaN HEMTs reliability is analyzed.

The HEMT AlGaN/GaN device used in this work had the epitaxial structure of a 17 nm unintentionally doped (UID) Al0.26Ga0.74N barrier layer, a 2 um UID GaN buffer layer and 1 um silicon substrate. The device had a gate length of 0.65 um, while source and drain length of 2 um respectively. Over the device, a 400 nm thick AlN layer as passivation was deposited within source and drain along 5 um. In this structure, ideal metal contact on source, drain and gate was assumed

Figure 1. HEMT AlGaN/GaN structure with AlN passivation.
Figure 2. Simulation result of lattice temperature compared with the experimental data as reference [2].

For simulation model calibration, another device having the same epitaxial structure but with gate length of 2.5 um, a 12.5 um separation between source-drain and without passivation layer was simulated under $V_{gs}=0V$ and $V_{ds}=30V$. The simulation result as shown in Fig. 2 indicates the lattice temperature distribution of AlGaN barrier layer is close to the experimental data with good agreement [2].

Besides thermodynamic model, other models are used to predict the device performance such as the Canali model drift velocity, the SRH recombination model, and Schroedinger-Poisson coupled solver to simulate the phenomenon in the 2DEG region accurately [8-10].

III. SIMULATION RESULT AND DISCUSSION

Figure 3 demonstrates the comparison of lattice temperature of AlGaN/GaN HEMTs in the presence and absence of AlN passivation on the device at zero bias condition and 30 V of drain voltage. The hot spot appeared at the same location at the edge of the gate. Furthermore, the lattice temperature distribution of the device with AlN passivation was more uniform than unpassivated devices. The lattice temperature profile curve at AlGaN/GaN active layer as shown in Fig. 4, describes a significant reduction of maximum lattice temperature by using AlN material as passivation.

The vertical electric field in case of unpassivated device as shown in Fig. 5(a) is higher compared to unpassivated device Fig. 5(b). When a high vertical electric field is applied through the AlGaN layer under higher bias conditions the stress increases as a result of the strong piezoelectric nature of AlGaN and GaN degrading the performance of the device.

The correlation between the lattice temperatures and vertical electric field with the planar stress can be seen in Fig. 6(a) and with the elastic energy is shown in Fig. 6(b). The rise in temperature at the same level of electric field reduces the planar stress and elastic energy of AlGaN/GaN HEMTs. Thus, the device reliability can be improved.

Thereby, these electrical, thermal, and mechanical properties are critical points in influencing the reliability of AlGaN / GaN HEMTs performance.
The stress mechanism on AlGaN/GaN HEMT is temperature dependent, this correlation is written by \[11\].

\[
\sigma = \sigma_i + \sigma_{th}
\]  

Where, \(\sigma_i\) is Intrinsic stress and \(\sigma_{th}\) is thermal stress which is given by,

\[
\sigma_{th} = \frac{E_2(\alpha_1 - \alpha_2)(T - T_0)}{(1 - \nu_2)}
\]

Where, \(E_2\) is Young’s modulus, \(\alpha_1\) and \(\alpha_2\) is expansion thermal coefficient of GaN and AlGaN layer respectively, \(\nu_2\) is Poisson’s ratio, and \(T_0\) is growth temperature.
Figure 8. Current density profiles in AlGaN/GaN layer (a) Unpassivated and (b) with AlN passivation under On-state condition.

Moreover, the uniform lattice heating on 442 K also decreased the elastic energy by ~20% both in on and off state condition.

Figure 8 shows the current density profiles of the simulated HEMTs without and with AlN passivation layer, respectively biased in the on-state condition. The data is compared for the same range and it is seen that the current density increases in the case of passivated device. The dc characteristics of the two devices are shown in Fig. 9. The drain current in case of AlN passivation increases by a significant percentage around 30% in agreement with the reference paper [5]. Also, the knee walkout observed in the case of unpassivated device which implies current collapse is suppressed by using AlN passivation layer.

The surface states captures the electrons injected from the gate electrode under higher bias conditions between the gate and drain electrodes. These trapped electrons reduce the 2DEG density due to charge neutrality and decreases the drain current [3]. It was observed that passivation results in lowering of the surface barrier and increase of the 2DEG density. For the increase in 2DEG at the interface, as well as compensate for the surface donor/acceptor state filling due to reduced surface barrier after passivation the layer must provide the positive charges to compensate the negative piezoelectric charge density at AlGaN surface [12].

IV. CONCLUSION

This paper presented electro-thermo-mechanical coupled analysis of AlN passivation layer over AlGaN/GaN HEMTs. AlN passivation layer over AlGaN layer effectively spread the surface heat from the channel resulting in reduction of the lattice temperature and induces an additional compressive stress. The drain current was significantly increased for the passivated device suppressing the current collapse. Thereby, AlN passivation layer enhances the electro-thermo-mechanical properties of AlGaN HEMTs.

REFERENCES


Development of ESD Robustness Enhancement of a Novel 800V LDMOS Multiple RESURF with Linear P-top Rings

Jung-Ruey Tsai¹²*, Yuan-Min Lee¹, Min-Chin Tsai¹, Gene Sheu¹², and Shao-Ming Yang¹
¹Department of Computer Science and Information Engineering, Asia University,
²Department of Photonics and Communication Engineering, Asia University
500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China
*e-mail: jrtsai@asia.edu.tw

Abstract—In this work, a novel 800V multiple RESURF LDMOS structures with or without P+ insertion region next to drain were developed to study the enhancement of ESD robustness. Compare to conventional RESURF LDMOS structures, the proposed multiple RESURF LDMOS without P+ insertion is able to achieve a specific on-resistance of lower than 130 mΩ⋅cm² while maintaining a breakdown voltage of over 800 volts. Furthermore, by using an additional P+ insertion next to drain, multiple RESURF LDMOS not only can improve the ESD robustness, which is demonstrated by the conventional 4 kV HBM testing but also increase the breakdown voltage higher than 900 volts. The thermal distribution of proposed structure was also studied under the ESD robustness testing using the thermodynamic mode simulation.

Keywords—ESD; Resurf; multiple rings; LDMOS; HBM

I. INTRODUCTION

Nowadays, reliability of an ultra high voltage LDMOS become the most leading issue in IC industry especially in ESD robustness. In many power management applications, ultra high voltage LDMOS is straightly connected to the pin. Therefore an on-chip ESD protection device should be established to ensure the ESD robustness of an LDMOS such that the ESD current can discharge efficiently [1,2]. It suggests that the development of enhancing the ESD robustness of high voltage LDMOS with various RESURF technologies has becoming more important [3-5]. The technology of ESD implant at drain side had been widely used in different LDMOS structures to get the better ESD robustness [4-7]. In addition, it had been demonstrated that the ESD robustness of conventional RESURF LDMOS can be improved by using the P+ insertion at drain side due to the excellence discharge ability of lateral Silicon Controlled Rectifier (SCR) formed by P+ region in the drain, N-drift region, P-well and N+ source regions. As a result, these two methods have worthy to implement in various LDMOS structures to study the ESD robustness. Besides, Technology Computer Aided Design (TCAD) tools are often used to simulate device ESD robustness such as the Human Body Model (HBM) test. Transient and circuit simulation are used in order to represent the HBM pulse. Thermodynamic method is used to accommodate the lattice temperature rising during the ESD stress. Physical models must be chosen carefully based on their dependence on lattice temperature in order to resemble the natural phenomena that happened during the ESD stress. Mesh design of simulated structure also plays an important role on the nodes elimination purpose in order to encounter TCAD nodes limitation while maintaining the doping profile and junction curvature. In this work, the simulation result shows that using P+ insertion at drain side can help the discharge of ESD current due to the additional current flow path. Even though ESD implant and P+ insertion result in the similar enhancement on ESD robustness, P+ insertion doesn’t need additional mask and process compared to ESD implant, therefore P+ insertion is a better choice to enhance the ESD robustness without extra fabricating cost.

II. DEVICE STRUCTURES AND CHARACTERIZATION

A. Design of Device Structure

Based on our previous work on the linear doping gradient by multiple-windows mask design to perform N-drift region to obtain the optimal electric field distribution [8], Fig. 1 (a) shows schematic cross-sections of a novel 800V high-voltage multiple RESURF N-LDMOS with the round shaped P-type rings in the top of N-drift region implemented by the conventional process simulator of TSUPREM4. The background doping of <100> oriented silicon substrate was p-type concentration of $1\times10^{14}$ cm⁻² and P-well doping was about $5\times10^{19}$ cm⁻³. In order to obtain a good trade-off between high breakdown voltage and specific on-resistance, a phosphorus dose of $2.9\times10^{12}$ cm⁻² was implanted to perform the N-drift region at 580 keV and the mask design of p-type rounded-rings was performed using analytical calculation to get a linear gradient doping profile in the top of drift region, as shown in Fig. 1 (b). In addition, high dose phosphorus implantation was used to perform the source and drain regions at doses of $1\times10^{15}$ cm⁻² at 100 keV and $3\times10^{15}$ cm⁻² at 400 keV, respectively to reduce the contact resistance. As device happened at breakdown condition, the P-top rings and N-drift regions should be depleted completely.

This research is funded in part by Vanguard International Semiconductor Corporation, Taiwan, Republic of China.
B. Considerations of Device Electrical Characteristics

Figure 2 compares the electric field distributions in three different RESURF technologies of LDMOS at device breakdown. Compare to single RESURF structure, the double RESURF one can reduce the maximum electric fields in the critical regions of drain side and gate edge near the drain. Obviously, structure with linear P-top rings can further reduce more electric field to get more uniform electric field distribution. As the drain bias increases, the depletion layer of drift region will be widened until it punches through to the P-top rings. Under the effect of electric field caused by the P-top rings generating negative charges which introduce additional electric fields with direction opposite to the intrinsic electric fields, the peak electric field of the main junction edge is reduced. It is reasonable that holes in P-top rings have flowed into main junction (N-drift/P-body junction) after the depletion layer of n-drift region reaches the P-top rings which may affect the P-top rings becoming non-neutral. Furthermore, at the edge of each ring, the introduced negative charges will create a new peak electric field as shown in Fig. 2. By optimizing the spacing and width of each ring, the breakdown voltage is increased since the electric fields can be well distributed in new introduced electric field peaks which are smaller than the silicon critical electric field. It means that the P-top RESURF LDMOS structure is easier to reach fully depletion in drift region as the device operated at higher breakdown voltage as compare to devices with conventional RESURF technologies.

In order to obtain the optimal Baliga’s figure of merit (BFOM), the breakdown voltage and on-resistance had been simulated at different lengths (L_p) from P-top rings to the N-drift junction under the gate region as shown in Fig. (3). It clearly shows that the on-resistance was decreased with the decreased L_p length due to the crowed electric charges under the gate region which results in the decrease of effective current path in the drift region. As the L_p length is larger than 4μm, the on-resistance will be saturated while the breakdown voltage will be decreased due to the increase of electric field near the drain side of the current designations.

III. ESD ROBUSTNESS SIMULATIONS AND DISCUSSION

A. ESD Robustness Considerations

Figure 4 shows the simulation result of drain current vs. drain voltage of the multiple RESURF LDMOS structure using the human body measurement (HBM) of 4 kV applied voltage by the conventional device simulator Medici to test its ESD robustness. The corresponding current flow in device was shown in Fig. 5. As device works after breakdown, the avalanche current induced by the strong electric field in junctions flow into the P+ region next to the source terminal resulting in a voltage drop (V_b) on the parasitic resistance (R_b) in the P-well. The first snapback behavior happened when the
parasitic PN junction between the source and P-well becomes forward bias to turn on its parasitic NPN bipolar as the \( V_B \) reaches high enough. In addition, the second snapback point suggests that an additional avalanche current induced by the strong electric field in junctions under the drain side. At the meantime, more carriers are injected into the drift region to cause LDMOS drain voltage decreases continually with the increased drain current. Consequently, the device can be burn out due to the continuous increasing drain current [9].

**B. Consideration of P+ Insertion effect on device**

Previous researchers had been suggested that there are some solutions can be implemented to improve the LDMOS ESD robustness characteristics such as to decrease the parasitic resistor by adjusting the P-well doping and to insert the P+ region next to the drain side [4]. By the way the drain current at the snapback point can be higher to get better discharge ability. However, the P-well doping adjustment is the most critical engineering strongly effects on device characteristics which cannot be modified arbitrarily. As a result, this work also provides a novel multiple RESURF structure using the P-top rings combined with the additional P+ region insertion next to the drain size, as shown in Fig. 6.

Figure 7 (a) clearly shows that the avalanche occurs firstly under the drain edge for the device without P+ insertion next to the drain. The parasitic vertical PNP will be turned on as the voltage drop on \( R_{N-drift} \) is increased due to the increase of avalanche current which results in the discharge current mainly flow laterally to the P+ bulk contact near source, and partly flow vertically through parasitic PNP, as shown in Fig. 7 (b). Once the voltage drop on \( R_{N-drift} \) is increased enough, the vertical PNP will be turned on and an additional discharge path will be performed to reduce the current density at the source, as shown in Fig. 7 (c). As a result, it is hard to get an enough voltage drop on base resistor to turn on the lateral parasitic NPN by insertion the P+ region next to the drain.

In addition, compare to Fig. 3, Figure 8 shows that the proposed multiple RESURF P-top rings LDMOS structure with an additional P+ region insertion next to drain has higher breakdown voltage closed to be about 900 V. This can be attributed by more depletion areas near the drain side results in the higher on-resistance, which was evaluated to be about 165 m\( \Omega \)-cm\(^2\). Figure 9 shows the ESD robustness test using the 4KV HBM circuit simulation by Medici. Both of the first and
second snapback voltages can be decreased due to the insertion of P+ region next to the drain. In addition, the inset indicates that the location of hot spot was occurred at the drain side and the maximum lattice temperature just only about 310 K using by thermal dynamic mode simulation. This suggests that our proposed structure not only contributes an easy method to enhance the device ESD robustness but also provides a excellent thermal reliability for power LDMOS.

IV. CONCLUSIONS

This paper proposed a novel 800V multiple RESURF LDMOS structures with or without P+ insertion region next to drain to study the ESD robustness enhancement. By adjusting the doping concentrations an mask locations, the low on-resistance and high breakdown voltage can be reached to their optimal values. In addition, the parasitic vertical PNP will be easily turned on as the voltage drop on R_N-drift is increased due to the increase of avalanche current by the insertion of P+ region. As a result, the improved ESD robustness, higher breakdown voltage and good thermal reliability performances can be easily achieved by using an additional P+ insertion next to drain in our proposed multiple RESURF LDMOS structure.

ACKNOWLEDGMENT

We are grateful to the National Center, Taiwan in supporting the High-performance Computing for computer time and facilities. In addition, we would like to thank Vanguard International Semiconductor Corporation, Taiwan for great supporting and helpful discussion.

REFERENCES

Design of Multiple RESURF LDMOS with P-top rings and STI regions in 65nm CMOS Technology

Yuan-Min Lee¹, Gene Sheu¹², Shao-Ming Yang¹, and Jung-Ruey Tsai¹²*  
¹Department of Computer Science and Information Engineering, Asia University,  
²Department of Photonics and Communication Engineering, Asia University  
500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China  
*e-mail: jrtsai@asia.edu.tw

Abstract—In this work, a novel multiple RESURF P-top rings LDMOS with shallow trench isolation (STI) structure based on the 65 nm baseline low-voltage CMOS technology by three-dimensional Sentaurus process and device simulations. A optimized uniform electric filed distribution in N-drift region can be obtained by employing the multiple P-top rings process instead of the past proposed gate field plates method in the extended drain regions. By this way, not only both of high breakdown voltage exceeded over 40V and low on-resistance below 20 mΩ-mm² can be achieved, but also the effect of Ws/dof/WSTI ratio on device can be reduce to obtain the larger optimal window of device characteristics, as compared with the conventional DIELER and graded gate field plate devices.

Keywords—RESURF; multiple P-top rings; LDMOS; STI; BFOM; DIELER; gate field plate

I. INTRODUCTION

Development of battery-powered system-on-chip (SoC) circuits with high gate voltage in the sub-100nm CMOS process technology is getting more important to meet the functionality requirements of portable electronic device applications [1, 2]. The Bipolar-CMOS-DIOMOS (BCD) integrated of high-voltage devices features such as embedded power management functions must be implemented without additional mask steps and process cost [3]. Their applications including display driver circuitry, and embedded flash memory drive circuit, for example: the voltage level translator, or charge pump. Therefore, in order to solve the next generation of display output circuit drives for the liquid crystal emitting diode (OLED) require the implement of low-voltage complementary NMOS/PMOS devices [4, 5].

Extended drain MOS (EDMOS) transistors [6] typically suffer severe HCl degradation in obtained high voltage processes is rectified optimization process but only with limited breakdown voltage. The DIELER device concept [7] of high-voltage capability can be enhanced with a STI/active stripe geometry in the drain extension. The devices applied the poly fingers on top of STI regions can be used as lateral field plates and other hybrid HV_GS/HV_DS device [8-10] used STI-sidewalls along vertical planes to enables flexible optimization in multiple voltages. However, additional processing steps do not meet the general requirements in the standard CMOS process technology. In addition, double and multiple RESURF methods [11, 12] had been developed instead of single RESURF technology to improve the junction/weak avalanche leakage at high electric field regions and reduce hot carrier injection into the dielectric in the aims of obtaining high breakdown voltage and low specific on-resistance requirements in conventional N-LDMOS devices. By adding an additional P-type layer in the top of N-drift region, the specific on-resistance can be decreased but the improvement of breakdown voltage is limited.

In this work, a novel multiple RESURF P-top rings with STI-sided N-LDMOS device is developed to realize a high breakdown voltage, low on-resistance, good charge balance sensitivity based on 65nm baseline low-voltage CMOS technology which is demonstrated by using three-dimensional Sentaurus process and device simulators. By tuning not only the doping concentration in substrate, N-drift and multiple P-top rings regions, but also the width ratio of N-drift region divided by STI one (Ws/N-drift/WSTI), a low specific on-resistance below 20 mΩ-cm² while maintaining a high breakdown voltage over 40 volts can be achieved successfully in this work.

II. DEVICE STRUCTURES AND CHARACTERIZATION

A. A novel Multiple P-top rings LDMOS Structure with STI

Figure 1(a) shows the schematic of a novel 3-dimensional and multiple P-top rings RESURF LDMOS structure with STI regions on both sides of the N-drift region which is performed by Sentaurus process simulation. Figure 1 (b) to (c) show the front, side and top views, respectively. It clear shows that the multiple P rings is performed in the top of the N-drift region. Because the minimal ring size is limited by the design rule of mask standards based on the basic process of 65 nm CMOS technology, the amount of P-top rings were designed to be five implemented into N-drift region to obtain the linear doping profile under electric field balance consideration, as shown in Fig. 2. In addition, mask numbers of this device were the same as the proposed advanced EDMOS transistor, being compared in this work [3]. For process conditions, the p-type background doping of about 7×10¹⁴ cm⁻³ was used in a <100> oriented silicon substrate. An epitaxial process of 0.7-μm-thickness N-type layer was performed on Si substrate with a doping concentration around 7×10¹⁶ cm⁻³. In order to obtain a good trade-off between high breakdown voltage and specific on-
resistance, the mask design of p-type rounded-rings with a implanted dose of about $1 \times 10^{12}$ cm$^{-2}$ was performed using analytical calculation to get a linear gradient doping profile in the top of drift region. It makes sure that as the device breakdown happened, the depletion regions were filled in the P-top rings and N-drift layer. In addition, a variety of substrate doping and the width ratio of $W_{N\text{-drift}}/W_{STI}$ were applied to obtain the optimal Baliga’s figure of merit (BFOM).

B. Considerations of Device Electric field distributions

Figure 3 illustrates the electric field distribution of the newly proposed device. The maximum of electric field was occurred in the junction between the largest P-top ring and N-drift region near the gate side for the $W_{N\text{-drift}}/W_{STI}$ width ratios equal to 0.25 and 0.43 at the substrate doping of $6 \times 10^{16}$ cm$^{-3}$. It clearly shows that the peak of electric field is increased with the decreased width ratio of $W_{N\text{-drift}}/W_{STI}$ and the electric field profile can be extended toward the drain side. The wider STI regions or narrower silicon regions had been proposed to contribute better high voltage capability [3, 9]. However, more uniform electric field distributions cannot be obtained by reducing the $W_{N\text{-drift}}/W_{STI}$ width ratio according to the trend of electric field profiles caused by the variation of $W_{N\text{-drift}}/W_{STI}$ ratio due to the limitation of device dimension. It implies that the maximum breakdown voltage of the newly proposed device is weak function of the ratio of $W_{N\text{-drift}}/W_{STI}$. As a result, the more uniform electric field can be obtained by tuning both of the substrate doping and P-top rings doping, as shown in Fig. (3). In addition, compared with the past proposed EDNMOS, DIELER and NMOS devices [3] with graded gate field plates (GFP) structures, the balance of electric field in the N-drift region can be easily obtained by using the multiple RESURF P-top rings. In addition, it is reasonable to suggest that the bulk current originated from avalanche generated hot carriers can be suppressed due to the reduction electric field in the junction near the gate edge, as shown in Fig. 4.
III. SIMULATIONS AND DISCUSSION

A. Device breakdown and Current flow path

Figure 5 shows the drain current versus drain voltage characteristics as the device operated at the off-state condition for the structure with the $W_{N-drift}/W_{STI}$ width ratio of 0.42. As the drain bias increases, the depletion layer of drift region will be widened until it punches through into the P-top rings. Because additional electric fields generated by the depletions near the P-top rings in the N-drift region, the peak electric field near the gate edge was reduced and the overall electric field distributions moved toward the drain size. The excellent electrical performance of device appeared that the high breakdown voltage was exceeded over 40V and the low leakage current was below $1 \times 10^{-12}$ amp which can be comparable to the device characteristics of the past proposed devices. Figure 6 (a) and (b) present the corresponding cross-section views of current flow distributions in the silicon region and STI, respectively as the newly proposed device at breakdown. It clearly demonstrated that the STI regions can confine the main current flow along with the surface of P-top rings towards to the source, not under the STI. Furthermore, on-resistance of device will be increased reasonably with the wider STI regions due to current crowding effect by the narrower current path.

B. Optimized Characteristics of Device

In order to obtain the optimal BFOM value, Fig. 7 shows the off-state breakdown voltage and on-resistance curves as a function of the ratio of $W_{N-drift}/W_{STI}$. It clearly appears that the breakdown voltage can be reached to 46V and the degradation of breakdown voltage is a weak function of $W_{N-drift}/W_{STI}$ ratio. Furthermore, the on-resistance of this newly proposed device can be improved more 30% as the $W_{N-drift}/W_{STI}$ ratio varied from 0.42 to 2.33. The lowest on-resistance of this device can be reached to about 17 $\Omega \cdot \text{mm}^2$. In addition, the inset in Fig. 7 compares the breakdown voltage of this device with that of the past proposed power devices. The optimal breakdown voltage of DIELER and GFP devices is about 35 V, which is lower than that of this proposed device with multiple P-top ring and STI structure, which also provides a larger optimal window of breakdown voltage defined as the 10% variation of breakdown voltage by $W_{N-drift}/W_{STI}$ ratio, as shown in shadow areas.

It well known that the junction and avalanche leakage currents strongly affect the device reverse off-state characteristics at high electric fields. In conventional DIELER device, STI regions can spread the electric field by decreasing the drain-extended region doping. By implementing the gate fingers on STI regions, the depletion of the drain-extended regions can be enhanced by the increase of optimal surface potential distributions to get more uniform electric field distributions between gate and drain sides. As a result, the $W_{N-drift}/W_{STI}$ ratio significantly influences the device breakdown. However, the balanced electric field between the gate edge and drain side is hard to achieve in such devices due to device geometry consideration. Therefore, multiple P-top rings were employed in this work instead of the conventional gate field plate design to reduce efficiently the electric field at gate edge and get more uniform electric field distribution in the drain-extended regions, as shown in Fig. 3.
Figure 8. Characteristics comparison of our novel multiple RESURF P-top rings/STI N-LDMOS with other advanced DIELER, graded GFP HV-NMOS transistors and various existing technologies.

Figure 8 shows the device performance criterion judged by the high breakdown voltage and low on-resistance of various devices in their optimized process conditions. It clearly demonstrated that the novel LDMOS using the multiple RESURF P-top rings and STI can comparable with the past proposed high performance devices such as DIELER and Graded GFP devices [3].

IV. CONCLUSIONS

In order to meet the requirement of the 65nm baseline low-voltage CMOS technology, this paper proposed a state-of-the-art 40V LDMOS design using both the multiple P-top rings and STI regions demonstrated by three-dimensional Sentaurus process and device simulations. The multiple RESURF P-top rings was used to decrease the \( \frac{W_{N\text{-drift}}}{W_{STI}} \) ratio effect on device breakdown and increase the optimized window of device breakdown. The maximum breakdown voltage is about 46V and the on-resistance of this newly proposed device can be improved more than 50% as the \( \frac{W_{N\text{-drift}}}{W_{STI}} \) ratio varied from 0.42 to 2.33. In addition, the lowest on-resistance of this device can be reached to about 17 m\( \Omega \)-mm\(^2\). Based on these great electrical performances, we believe that this novel device has sufficient potential in comparable with previous advanced DMOS devices.

ACKNOWLEDGMENT

We are grateful to the National Center, Taiwan in supporting the High-performance Computing for computer time and facilities.

REFERENCES

[2] D. Riccardi et al., “BCD8 from 7V to 70V: a new 0.18 um Technology platform to address the evolution of applications towards smart power ICs with high logic contents”, ISPSD 2006, pp. 73-76.
SOI 横向超结器件表面势场分布三维解析模型

魏雪观1) 郭宇锋*1) 张长春1) 夏晓娟1) 许 健2)
1)(南京邮电大学电子科学与工程学院，南京 210003)
2)(亚洲大学资讯工程系，台中 413514)

本文基于三维泊松方程的求解，建立了 SOI 横向超结器件的表面电势和表面电场分布解析模型，并借助该模型和三维半导体仿真器件 DA VINCI，研究了随着 n 区和 p 区的浓度、长度、宽度、高度和埋氧层厚度等结构参数的变化，表面电势和表面电场的变化规律。最后，导出了一个 3D RESURF 判据，研究表明利用该判据进行器件设计可以获得最优的表面电场分布和最高的击穿电压。解析结果和 DA VINCI 数值仿真结果的一致性，验证的解析模型和 3D RESURF 判据的正确性。本文的工作为 SOI 横向超结器件的优化设计提供了理论指导。

关键词: SOI, 超结, 表面电势, 表面电场, 3D RESURF, 模型

1. 引言

众所周知，超结 (Super Junction) 结构打破了半导体功率器件耐压与导通电阻的极限关系，从而具有广泛的应用前景[1-2]。虽然基于超结概念的各种功率器件层出不穷，但是都可以归结为两大类: 纵向超结功率器件和横向超结功率器件。目前对于纵向超结功率器件的研究较为深入，特别是从理论上，人们提出了一系列电势电场分布模型和耐压模型[3-5]，较好地揭示了器件工作的物理机制，为结构设计和性能优化提供了强有力的理论指导。但是，对于横向超结器件而言，由于衬底辅助耗尽效应会形成相邻 p 区和 n 区电荷的不平衡，从而导致击穿电压急剧下降。为此，人们提出了各种技术来克服这一不足，如背部刻蚀技术[6-7]、非平

本文基于求解三维泊松方程，建立了 SOI 横向超结器件结构的三维解析模型，得出了表面电势和表面电场的解析表达式。利用三维器件仿真软件 DAVINCI 验证了模型的正确性。进一步，借助该模型和 DAVINCI 讨论了器件结构参数变化对表面势场分布和电荷平衡的影响，最终导出了一个 3D RESURF 判据，为揭示 SOI 横向超结功率器件的工作机理和进行结构参数的优化设计奠定了理论基础。

2. 解析物理模型

图 1 是 SOI 横向超结器件结构三维示意图，其中(a)为三维图，(b)为俯视图，可见超结结构是由周期性重复的 n 和 p 区组成。坐标系中 x 轴垂直于漂移区沿着 n 和 p 区方向界面， y 轴沿着漂移区界面， z 轴垂直埋氧层界面。图中$\tau_s$是顶层硅厚度(即 n 和 p 区的高度)，$t_{os}$是埋氧层厚度，W 为漂移区的长度(即 n 区和 p 区的长度)，b 为 n 区和 p 区的宽度，外加反向偏压$V_D$。由于其考虑其周期重复性和对称性，如图 1(b)两条虚线内的部分为我们考虑的范围。漂移区浓度分布

函数 $N(x,y,z)$ 为：

$$
N(x,y,z)=\begin{cases}
N_0, & 0 \leq x \leq b/2,-W/2 \leq y \leq W/2,0 \leq z \leq \tau_s \\
N_4,b/2 < x \leq b,-W/2 \leq y \leq W/2,0 \leq z \leq \tau_s 
\end{cases}
$$

其中 n 区杂质浓度为 $N_0$，p 区杂质浓度为 $N_4$。
当反向偏压 $V_D$ 足够大时漂移区全耗尽，耗尽区内电势 $\varphi(x, y, z)$ 满足以下的三维 Poisson 方程：

$$
\frac{\partial^2 \varphi(x, y, z)}{\partial x^2} + \frac{\partial^2 \varphi(x, y, z)}{\partial y^2} + \frac{\partial^2 \varphi(x, y, z)}{\partial z^2} = \frac{-qN(x, y, z)}{\varepsilon_{si}}
$$

其中 $q$ 为单位电荷，$\varepsilon_{si}$ 为硅介电常数。

由于漂移区表面电场的纵向分量远小于横向分量，并考虑到漂移区与埋氧层界面的电位移连续性，可以得到如下边界条件：

$$
\frac{\partial \varphi}{\partial z} \bigg|_{z=0} \approx 0
$$

$$
\varphi \bigg|_{z=t_{ox}} = -\frac{\partial \varphi}{\partial z} \bigg|_{z=t_{ox}} \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox}
$$

其中 $\varepsilon_{ox}$ 为埋氧层介电常数。

假设沿 $z$ 方向的电势满足抛物线分布$^{[12]}$，则耗尽区内电势 $\varphi(x, y, z)$ 满足：

$$
\varphi(x, y, z) = u(x, y) + v(x, y)z + w(x, y)z^2
$$

其中 $u(x, y)$ 为 $z = 0$ 时的表面电势，而 $v(x, y)$ 和 $w(x, y)$ 可由边界条件X(3)求出。

把X(3)和X(4)式代入X(2)式中，可把三维Poisson方程降维为二维Poisson方程：

$$
\frac{\partial^2 u(x, y)}{\partial x^2} + \frac{\partial^2 u(x, y)}{\partial y^2} - \frac{u(x, y)}{t^2} = \frac{-qN(x, y, z)}{\varepsilon_{si}}
$$

其中 $t = \sqrt{\frac{t_{ox}^2 + \varepsilon_{si} \varepsilon_{ox} t_{ox} t_{ox}}{2 \varepsilon_{ox} t_{ox}}} \varepsilon_{ox} t_{ox} t_{ox}$ 定义为漂移区本征厚度。

进一步，由于超结结构的周期对称性，图 1(b) 中 n 区和 p 区中线的边界条
件可以写为:
\[
\frac{\partial \phi}{\partial x}
\bigg|_{x=0} = 0
\]

（6）

为了求解方程X（5），将漂移区浓度\(N(x,y,z)\)进行如下的傅里叶变换:
\[
N(x,y,z) = a_0 + \sum_{n=1}^{\infty} a_n \cos\left(\frac{n\pi x}{b}\right)
\]

（7）

其中\(a_0 = \frac{N_D - N_A}{2}\)，\(a_n = 2 \frac{(N_D + N_A)}{n\pi} \sin\left(\frac{n\pi}{2}\right)\)，\(n = 1, 2, 3\ldots\)。

又考虑到方程X（5）的解\(u(x,y)\)应满足边界条件X（6），并且满足电势边界条件：\(\phi(x,-W/2,0) = V_D\)，\(\phi(x,W/2,0) = 0\)。于是\(u(x,y)\)可写成如下形式:
\[
u(x,y) = \sum_{n=1}^{\infty} u_n(y) \cos\left(\frac{n\pi x}{b}\right) + u_0(y)
\]

（8）

将X（8）代入X（5），并采用分离变量法，方程X（5）可进一步降维为如下的一维二阶常微分方程组:
\[
\begin{cases}
\frac{\partial^2 u_0(y)}{\partial y^2} - \frac{u_0(y)}{t^2} - \frac{q}{\varepsilon_{si}} a_0 = 0 \\
BC: u_0(-W/2) = V_D, u_0(W/2) = 0
\end{cases}
\]

（9）

\[
\begin{cases}
\frac{\partial^2 u_n(y)}{\partial y^2} - \frac{n^2 \pi^2}{b^2} u_n(y) - \frac{u_n(y)}{t^2} = -\frac{q}{\varepsilon_{si}} a_n \ (n = 1, 2, 3 \ldots)
\\
BC: u_n(-W/2) = 0, u_n(W/2) = 0
\end{cases}
\]

（10）

求解X（9）、X（10）式二维偏微分方程，得表面电势表达式为:
\[
\phi(x,y,0) = \frac{q}{\varepsilon_s} 2 \frac{(N_D + N_A)}{\pi^3} b^2 \sum_{n=1}^{\infty} \frac{1}{n^2 \theta_n^2} \sin\left(\frac{n\pi}{2}\right) \left[ 1 - \cosh\left(\frac{n\pi \theta_n}{b}\right) \cosh\left(\frac{n\pi \theta_n W}{2b}\right) \right] \cos\left(\frac{n\pi x}{b}\right)
\]

（11）

\[
+ \frac{q t^2}{\varepsilon_{si}} \frac{N_D - N_A}{2} \left[ 1 - \frac{\cosh\left(\frac{y}{t}\right)}{\cosh\left(\frac{W}{2t}\right)} \right] - V_D \frac{\sinh\left(\frac{1}{t} (y - \frac{W}{2})\right)}{\sinh\left(\frac{W}{t}\right)}
\]

其中\(\theta_n = \sqrt{1 + \frac{b^2}{\pi^2 n^2 t^2}}\)。

根据\(E_x = -\frac{\partial \phi}{\partial x}\)和\(E_y = -\frac{\partial \phi}{\partial y}\)可以计算出表面电场的\(x\)和\(y\)方向分量分别为:
\[ E_x(x, y, 0) = \frac{q}{\varepsilon_x} \frac{2(N_D + N_A) b}{\pi^2} \sum_{n=1}^{\infty} \frac{1}{n^2 \theta_n^2} \sin\left(\frac{n\pi x}{b}\right) \left[ 1 - \frac{\cosh\left(\frac{n\pi y}{b}\right)}{\cosh\left(\frac{n\pi \theta_n W}{2b}\right)} \right] \sin\left(\frac{n\pi x}{b}\right) \] (12)

\[ E_y(x, y, 0) = \frac{q}{\varepsilon_x} \frac{2(N_D + N_A) b}{\pi^2} \sum_{n=1}^{\infty} \frac{1}{n^2 \theta_n^2} \sin\left(\frac{n\pi x}{b}\right) \left[ \sin\left(\frac{n\pi y}{b}\right) \cosh\left(\frac{n\pi \theta_n W}{2b}\right) \right] \right] \sin\left(\frac{n\pi y}{b}\right) \] (13)

不难验证，当埋氧层的厚度无穷大时（即 \( \lim_{\theta_n \to \infty} = 1 \)），表面电势和表面电场分布表达式可以退化为文献[4]中表面电势和电场的表达式，这说明对耐压特性而言，纵向超结结构可以看作是 SOI 横向超结结构的一种特例（埋氧层厚度为无穷大）。

3. 结果与讨论

3.1. 三维表面势场分布的验证

为了验证模型的正确性，我们采用三维半导体器件 DAVINCI 对该结构进行数值仿真，图 2 给出了 SOI 横向超结器件表面电势和表面电场分布三维解析结果和模拟仿真结果。可见无论是电势分布还是电场分布，解析结果和仿真结果均吻合良好。对于表面电场分布而言，在阳极结和阴极结附近的解析结果比模拟结果稍大，这是因为在建模过程中，我们忽略阴极结和阳极结的曲率半径的影响，以及耗尽区在阴极区和阳极区内的扩展。进一步从图 2(a)中可以看出，表面电势沿漂移区长度方向变化明显，沿 n 区与 p 区宽度方向变化较小，但这并不意味着 SOI 横向超结器件的耐压问题仍然可以近似为二维问题，事实上从图 2(b)可以看出，无论在漂移区长度方向还是 n 区与 p 区宽度方向，表面电场分布均有剧烈变化。沿着漂移区长度方向，表面电场呈哑铃状。阴极结和阳极结界面上的表面电场最高，而中部表面电场比较低。而沿着 n 区与 p 区宽度方向情况比较复杂。在漂移区两端的峰值电场位于图 1 中的 \( A(0, \frac{W}{2}, 0) \) 和 \( B(b, -\frac{W}{2}, 0) \) 两点，在漂移区中间的峰值电场则位于 p 和 n 区交界处。
3.2. 结构参数对表面势场的影响

SOI 横向超结器件的结构参数的变化对表面势场的影响显著。在本节我们对 n 和 p 区浓度、埋氧层和顶层硅厚度、漂移区长度和 n 区与 p 区宽度等参数对 n 区和 p 区的交界面上表面势场影响进行讨论。

图 3 是 n 区和 p 区浓度变化对 n 区和 p 区的交界面上表面势场的影响。可见，无论 n 区 p 区浓度无何变化，表面电势和表面电场解析结果都可以与模拟结果较好地吻合。进一步，由图 3(a)(c)所示，该结构的表面电势降最大位置分别位于阴极结和阳极结附近，这表明横向耐压主要由阴极结和阳极结承担。此外，如图 3(b) (d)可以看出：随着 n 区浓度的增大或 p 区浓度的减小，阳极结附近的表面电场值增大；反之，随着 p 区浓度的增大或 n 区浓度的减小，阴极结附近的表面电场值增大。这种现象在常规的二维横向功率器件中也可以观察到，因此是一种典型的 RESURF 现象。
图 3 n 区和 p 区浓度变化对 n 区和 p 区的交界面上表面势场影响：(a) n 区浓度变化对表面电势的影响；(b) n 区浓度变化对表面电场的影响；(c) p 区浓度变化对表面电势的影响；(d) p 区浓度变化对表面电势的影响；(e) (f)（$N_d = 1 \times 10^{16} \text{ cm}^{-3}$, $V_D = 200V$）（c）p 区浓度变化对表面电势的影响；(d) p 区浓度变化对表面电势的影响；(e)（$N_d = 2.5 \times 10^{16} \text{ cm}^{-3}$, $V_D = 200V$）

图 4 是埋氧层和顶层硅厚度变化对 n 区和 p 区的交界面上表面势场的影响。由图可见，对于不同的埋氧层和顶层硅厚度，表面电势和表面电场的解析结果与模拟结果都比较一致。埋氧层和顶层硅厚度对表面势场分布的影响相反，埋氧层厚度增加或顶层硅厚度减小，可以降低阴极结表面电场，而提高阳极结表面电场；反之，埋氧层厚度减小或顶层硅厚度增大，可以提高阴极结表面电场，而降低阳极结表面电场。
图 4 埋氧层与顶层硅厚度变化对 n 区和 p 区的交界面上场势分布的影响：(a)埋氧层厚度变化对表面电势的影响；(b)埋氧层厚度变化对表面电场的影响（$N_D = 2.4 \times 10^{16} cm^{-3}$，$V_D = 200V$）；(c)顶层硅层厚度变化对表面电势的影响；(d)顶层硅层厚度变化对表面电场的影响（$N_D = 2.25 \times 10^{16} cm^{-3}$，$V_D = 200V$）

图 5 给出漂移区长度和 n 区与 p 区宽度变化对表面势场的影响。可见解析结果与模拟结果都能较好地吻合。进一步分析可发现，漂移区长度和 n 区与 p 区宽度的改变，不会影响 n 区和 p 区的交界面上的表面电势分布和两端的峰值电场，而仅仅改变了漂移区中部的表面电场。随着漂移区长度增加中部表面电场略有下降，而 n 区与 p 区宽度增加，导致中部表面电场的提高。
图 5 漂移区长度和 n 区与 p 区宽度变化对表面势场的影响：(a) 漂移区变化对表面电势的影响；(b) 漂移区变化对表面电场的影响；(c) $x = b/2$ 处 n 区与 p 区宽度变化对表面电场的影响；(d) $y = 0$ 处 n 区与 p 区宽度变化对表面电场的影响

3. 3 3D RESURF 判据

RESURF 判据最早是由 J. APPELS 在 1979 年对二维横向功率器件进行分析后提出的，由上节分析可知，SOI 横向超结结构体现出强烈的三维效应，如果继续采用传统的 RESURF 判据来进行设计，则会带来较大的误差，虽然人们提出了衬底辅助耗尽效等概念来解释这种不一致性，却无法进行定量的描述。本节提出一种全新的 3D RESURF 判据，作为对横向超结器件设计的理论指导。

由图 2 可知，当漂移区完全耗尽时，漂移区有两个峰值电场，即图 1(b) 中的即 $A(0, -W/2, 0)$ 和 $B(b, -W/2, 0)$ 点。对于优化的器件结构，当器件击穿时，这两点的电
场同时达到硅的临界电场 $E_c$，即 $E(0, \frac{W}{2}, 0) = E(b, -\frac{W}{2}, 0) = E_c$，将其代入X(12)与X(13)式中，可得最大击穿电压和临界电场分别满足:

$$V_{\text{max}}^b = \frac{qT^2}{\varepsilon_{si}} (N_D - N_A)$$

$$E_c = \frac{q(N_D + N_A)Wf_1}{2\varepsilon_{si}} + \frac{q(N_D - N_A)Wf_2}{2\varepsilon_{si}}$$

其中 $f_1 = \frac{4b}{\pi^2 W} \sum_{n=1}^{\infty} \frac{1}{n^2 \theta_n} \sin\left(\frac{n\pi}{2}\right) \tanh\left(\frac{n\pi\theta_n}{2b} W\right)$，$f_2 = \frac{t}{W} \frac{1}{\tanh\left(\frac{W}{2t}\right)}$。

这里 $f_1$ 函数可以用如下表达式来近似:

$$f_1 \approx 0.371 \frac{b}{\theta W}$$

图 6 对比了 $f_1$ 函数的精确和近似表达式，可见，在 $W/2b > 0.1$ 时，无论 $W/2t$ 如何变化，两者都非常一致。进一步分析，当埋氧层的厚度无穷大时，X(15)和X(16)式分别退化为文献[3]中的(8)和(10)式，这进一步说明了本文提出了模型不仅适用于SOI横向超结器件也适用于纵向超结器件。

为了获得器件结构最优时n区和p区浓度需要满足的条件，我们把X(16)式代
在SOI横向超结器件中漂移区长度要足够长，而且特征厚度也大于n区和p区的宽度，我们可以得到：

\[ N_D(t + 0.371b) - N_A(t - 0.371b) \approx \frac{2\varepsilon_s E_c}{q} \]

该式给出了对SOI横向超结器件进行设计的3D RESURF判据，该判据表明n和p区的浓度不仅取决于顶层硅和埋氧层的厚度，还取决于n区与p区宽度b。对于常规横向RESURF器件，我们令 \( N_A = -N_D \)，则X(17)式可以化简为

\[ N_D t \approx \varepsilon_s E_c / q \]

这就是Single RESURF器件的RESURF判据[13]。

图7给出了利用DAVINCI得到的最优的n区和p区浓度与最大击穿电压的数值模拟结果，以及由X(14)和X(17)式得到的解析结果，可见两者吻合较好。由此图可以看出，随着p区浓度\( N_D \)逐渐增大n区的优化浓度\( N_D \)也逐渐增大，但二者并不相等，这体现了SOI横向超结器件特有的衬底辅助耗尽效应，进一步比较该曲线与\( N_D = N_A \)直线的间距可知，随着\( N_A \)的增加，两者的间距减小，这说明衬底辅助耗尽效应逐渐减弱。
4. 结论

本文通过求解三维泊松方程，首次建立了 SOI 横向超结器件的三维物理模型，得出了表面电势和表面电场的解析表达式，并利用三维半导体器件 DA VINCI 验证了模型的正确性。进一步，借助该模型和 DA VINCI 深入讨论了器件结构参数变化对表面电势和表面电场分布的影响。研究表明，本模型可以准确的定量分析 n 区杂质浓度、p 区杂质浓度、埋氧层厚度、顶层硅厚度、漂移区长度、n 区和 p 区的宽度等各种参数对表面势场的影响。最终，我们导出了一个新的 3D RESURF 判据，该判据不同于常规的 Single 和 Double RESURF 判据，它定量地揭示了 SOI 横向超结器件的三维耐压机理，为优化器件结构参数、提高击穿电压提供了理论指导。

参考文献:


A three dimensional analytical model of surface potential and electric field distributions for SOI lateral super junction devices

Xueguan Wei†1, Yufeng Guo†1), Changchun Zhang1, Xiaojuan Xia1, Gene Sheu2

1)(Electronic Science & Engineering, Nanjing University of Posts and Telecommunications, Nanjing 210003, Jiangsu)

2)(Computer Science and Information Engineering Department Asia University Taichung, 413514, Taiwan)

Abstract

Based on solving the 3-D Poisson’s equation, we propose a 3-D analytical model of the surface potential and the surface electric fields distributions for the SOI lateral SJ (Super Junction) device. Then, the proposed analytical model and the 3-D semiconductor simulator DAVINCI are used to study the variation of the surface potential and the surface electric fields with the change of device parameter including the doping concentration, length, width and height of the p-pillar and n-pillar, as well as the buried oxide thickness. Finally, a 3D RESURF criterion is derived to optimize the surface field distribution and maximize the breakdown voltage. The proposed model and the 3D RESURF criterion are verified by the fair agreements between the analytical results and numerical simulations by DAVINCI. This paper contributes an efficient and time-saving scheme for the design of SOI lateral SJ device.

Key words: SOI, super junction, surface potential, surface electric field, 3D RESURF, model

PACC: 7340L

PACS: 85.30.De, 85.30.TV

† Email: yfguo@njupt.edu.cn

We thank the financial support by National Natural Science Funds of China (No. 60806027, No. 61076073) Foundation of State key Laboratory of Electronic Thin Films and Integrated Devices(No. KFJJ201011), and Foundation of Jiangsu Educational Committee (No. 09KJB510010)
2012 International Workshop on Information and Electronics Engineering (IWIEE 2012)

A Novel RF SOI LDMOS with a Raised Drift Region

Qin Xu\textsuperscript{a}, Yufeng Guo\textsuperscript{a}, Ying Zhang\textsuperscript{a}, Leilei Liu\textsuperscript{a}, Gene Sheu\textsuperscript{b}, Jiafei Yao\textsuperscript{a}, *\textsuperscript{a}

\textsuperscript{a}Nanjing University of Posts and Telecommunications, Nanjing 210003, China
\textsuperscript{b}Asia University, Taichung, Taiwan, China

Abstract

In this paper, we propose a novel RF SOI LDMOS with a raised drift region (RDR). Using the process simulation and numerical simulation, we investigate deeply on breakdown characteristics and frequency characteristics of this novel device. Compared with the conventional RESURF device, the breakdown voltage and cutoff frequency of the RDR device are increased by 25\% and 21\%, respectively. The work of this paper has theoretical and practical significations to the research of a new generation of deep sub-micron high-performance radio frequency SOI integrated circuits.

© 2011 Published by Elsevier Ltd. Selection and/or peer-review under responsibility of [name organizer]

Keywords: RF; SOI LDMOS; Raised Drift Region; breakdown voltage; cutoff frequency

1. Introduction

Laterally double diffused metal oxide semiconductor (LDMOS) technology is one of the most attractive technologies deployed in RF power amplifier applications because of its ease in integration to standard CMOS technology, high input impedance at high drive current and thermal stability \footnote{[1]}. Especially, silicon on insulator (SOI) LDMOS is more attractive due to its inherent dielectric isolation, high frequency performance and reduced parasitic capacitance \footnote{[2-3]}. In recent years, many researches focus on optimizing structures to improve breakdown voltage, reduce on-resistance and increase cutoff frequency and maximum oscillation frequency \footnote{[4-8]}.

In this paper, we propose a novel RF SOI LDMOS device with an RDR (Raised Drift Region) to improve breakdown characteristics and frequency characteristics. This novel device can be fabricated by using the deep sub-micron CMOS compatible process with an additional LOCOS process to form the

* Corresponding author. Tel.: +86-025-85866321; fax: +86-025-85866321.
E-mail address: yfguo@njupt.edu.cn.
raised drift region. The paper is organized as follows. In section II, the concept of the RDR structure and its fabrication process is proposed. In section III, the breakdown characteristics and frequency characteristics of the RDR device is investigated compared with the conventional RESURF device. Section IV gives a summary of conclusions.

2. Device structure and process

A cross section of the RDR RF SOI LDMOS structure is shown in fig. 1(a). In comparison with the conventional RESURF device, the RDR device has a special drift region with the vertical thickness increasing gradually from the source side to the drain side.

Fig. 1. The RDR RF SOI LDMOS device: (a) cross section; (b)-(e) process steps.

Fig. 1(b)-(e) illustrates the process flow of the RDR device. The proposed process of the RDR device is simulated with 2D process simulator Tsuprem4. The doping concentration of the n-type SOI wafer is $1 \times 10^{16}$ cm$^{-3}$. First, LOCOS process is used to fabricate the raised drift region. The oxidation steps were carried out in wet O$_2$ ambient at 1000°C for 97 minutes, as shown in fig. 1(c). Then, a boron implantation of $3 \times 10^{13}$ cm$^{-2}$ dose and 15KeV energy was diffused to form the p-well which is diffused for 10 minutes at 1000°C. The gate oxide and the poly silicon gate were deposited and etched as shown in fig. 1(d). An arsenic implantation of $2 \times 10^{15}$ cm$^{-2}$ dose and 25KeV energy was used to create the source and drain regions. Finally, the field oxide was deposited and the metal contact holes were fabricated as shown in fig. 1(e).

3. Simulation results and discussion

2D device simulator MEDICI is employed to investigate the characteristics of the proposed RDR device and conventional RESURF device with same physical dimensions. Table 1 gives the basic geometric parameters of these devices.

Table 1. Device parameters used in simulation.
3.1. Breakdown characteristics

Fig. 2(a) shows the breakdown voltage as a function of the drift doping dose for the RDR and conventional devices. The breakdown voltage of both devices first increases slowly then falls rapidly with the increase of the drift region’s dose. As shown in the figure, the maximum breakdown voltage of the RDR structure is 19.9V, increased by 25% compared with the conventional device. To further explore the breakdown mechanism of the RDR device, fig. 2(b) gives the surface electric field of both devices when the breakdown voltage is maximized. For the conventional RESURF device, the surface electric field is highest near both ends of the drift region while it is minimal on the central part of the drift region. On the contrary, the RDR structure provides a more uniform surface electric field. The reason is that the RDR device optimizes the surface charge density to be close to the linear distribution, which is very favorable to increase the horizontal breakdown voltage as in VLD devices [8]. Furthermore, an obvious reduction in the electric field peak of P-well/N-drift and N-drift/N⁺-drain junctions can be seen in the fig. 2(b). The P-well/N-drift junction of the RDR device is a negative bevel compared with the conventional RESURF device, as shown in fig. 3. Since the negative bevel removes more charge from the P-side of the junction than the N-side, the depletion region expands on the P-side and contracts on the N-side at the surface, which could cause a reduction of the surface electric field [9].

![Graphs showing breakdown voltage and surface electric fields](image-url)
3.2. Frequency characteristics

For RF LDMOS devices, the gate-source capacitance $C_{gs}$ and gate-drain capacitance $C_{gd}$ are the most relevant intrinsic capacitances affecting the cutoff frequency $f_t$ [10]. Fig. 4 illustrates $C_{gs}$ and $C_{gd}$ as a function of the drain voltage for the RDR and conventional devices. $C_{gs}$ of the RDR device is smaller than the conventional one by 10% in the Fig. 4(a). However, $C_{gd}$ of the RDR device increases 23% compared with the conventional one. The reason is that the negative bevel P-well/N-drift junction in the RDR device leads to a smaller depletion width in the drift region [9].

![Fig. 4](image)

**Fig. 4.** Simulation results for capacitance comparison between RDR and conventional devices using the small signal method, at frequency 1MHz and $V_{ds} = 7V$: (a) gate-drain capacitance; (b) gate-source capacitance.

![Fig. 5](image)

**Fig. 5.** Comparison of conventional and RDR devices at frequency 1MHz and $V_{ds} = 7V$: (a) transconductance; (b) cutoff frequency.
Although suffering from an intrinsic drawback of higher $C_{gd}$, the RDR device poses superior transconductance characteristics compared with the conventional device. As shown in fig. 5(a), the transconductance of the RDR device increases 33% compared with the conventional one because the novel device can effectively adjust the electric field distribution of the drift region. One of the figures of merit of a RF power device is the cutoff frequency in high-frequency operation. It is defined by the frequency at which the input current becomes equal to the load current [11]. Fig. 5(b) shows the simulation results of the comparison between the cutoff frequency and gate voltage for the RDR and conventional devices at $V_{ds}=7V$. The cutoff frequency of the RDR device is 18.6GHz and increases 21% compared with the conventional one. Thanks to the superior transconductance characteristics, the RDR structure still has the comparable frequency performance in despite of the higher $C_{gd}$.

4. Conclusions

This paper proposes a novel RF SOI LDMOS device with a Raised Drift Region that can be fabricated by an additional LOCOS process in the deep sub-micro CMOS process. The 0.18µm gate length promises a record cutoff frequency of 18.6GHz and a high breakdown voltage of 19.9V. According to the numerical simulation results by TSUPREM4 and MEDICI, the proposed device is demonstrated to exhibit improved breakdown voltage (by 25%) and cutoff frequency (by 21%) compared to the conventional RESURF device. Therefore, the proposed RDR device is a promising candidate in the area of RF integrated circuits.

Acknowledgements

We thank the financial support by National Natural Science Funds of China (No. 60806027, No. 61076073) Foundation of State key Laboratory of Electronic Thin Films and Integrated Devices(No. KFJJ201011), and Foundation of Jiangsu Educational Committee (No. 09KJB510010).

References


A New Methodology to Investigate the Effect of Stress and Bias on 2DEG and Drain Current of AlGaN/GaN Based Heterostructure

Manoj Kumar\textsuperscript{a}, Gene Sheu\textsuperscript{a,b}, Jung-Ruey Tsai\textsuperscript{a,b,*}, Shao-Ming Yang\textsuperscript{a}, and Yu-Feng Guo\textsuperscript{c}

\textsuperscript{a} Department of Computer Science and Information Engineering, \\
\textsuperscript{b} Department of Photonics and Communication Engineering \\
Asia University, 500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, R. O. C. \\
\textsuperscript{c} School of Electronic Science and Engineering, Nanjing University of Posts and Telecommunications \\
Nanjing, Jiangsu, 210096, China \\
*e-mail: jrtsai@asia.edu.tw

The effect of negative, neutral and positive stress by Si$_3$N$_4$ film on AlGaN layer of AlGaN/GaN based high electron mobility transistor (HEMT) heterostructure has been investigated by varying different stress values using Synopsys Sentaurus device simulation. This paper shows a relation between the stresses of passivation layer, two dimensional electron gas (2DEG) formed at the interface of AlGaN/GaN region and respective drain current. The increase in negative stress will result in the increase of 2DEG density, which will result in the increase of drain current. Additionally, the 2DEG density was found to be depended on the applied bias voltage, showing the higher drain sweep voltage will increase the 2DEG density. This study also provides the effect of stress on direct-current (DC) capacitance-voltage characteristics of device electrical performance. It suggests that the capacitance will be increased with the increasing positive stress, indicating the change in interface states due to stress effect.

Introduction

AlGaN/GaN based high electron mobility transistors (HEMTs) are intensively studied due to their potential use in high frequency, high power and high temperature applications (1-4). Since device possess excellent characteristics suitable for these applications such as wide band gap of 3.4eV, larger breakdown electric field (3MV/cm) and large two dimensional electron gas (2DEG) concentration close to 10$^{13}$ cm$^{-2}$ at the interface region of AlGaN/GaN without additional doping (5). Such a high 2DEG concentration is very difficult to achieve in other III-V material based device (6). Several good methods have been developed to understand the nature of 2DEG region of AlGaN/GaN based HEMTs to improve the reliability of these devices. One of such method is Si$_3$N$_4$ surface passivation layer over the AlGaN/GaN HEMT (7-9). Induction of Si$_3$N$_4$ passivation minimizes the effect of surface traps and removes the depletion of 2DEG by providing more positive charge at 2DEG (10, 11).
In this paper, we have investigated the effect of different stress conditions on Si$_3$N$_4$ surface passivation layer and compared with neutral condition by TCAD simulation. Our investigation shows that 2DEG region concentration changes with different stress condition. In our work we found that 2DEG concentration exhibits linear characteristics with different stresses. Additionally, we investigated the drain current for all conditions of stress and found a linear relationship between drain current and 2DEG concentration for different drain bias conditions.

**Device Overview**

Figure 1 shows the device structure of AlGaN/GaN heterostructure which is grown over P+ doped Si substrate. The doping concentration of Si substrate is $1 \times 10^{16}$/cm$^2$. Device consists of 2$\mu$m thick undoped GaN layer above this layer 17nm thick undoped Al$_{0.26}$Ga$_{0.74}$N barrier layer is deposited (12). For source and drain contacts Al/Ti (0.1/0.1 $\mu$m) material was used and ohmic contact was formed. For Schottky gate contact Au/Pt (0.1/0.1 $\mu$m) material is used. The thickness of Si$_3$N$_4$ surface passivation is 0.4 $\mu$m.

![Figure 1. Cross sectional view of undoped AlGaN/GaN structure with 0.4$\mu$m thick Si$_3$N$_4$ passivation layer.](image)

**Results and Discussion**

The Simulation is done using Synopsys Sentaurus device simulator. The device is made using the TCAD tool sentaurus device editor and for induction of stress sprocess tool is used. Figure 2 shows stress distribution of negative and positive stress ($\pm3$GPa) along XX direction for the given device. Stress affects the 2DEG density at the AlGaN/GaN interface. In this stress test we measure 2DEG dose in the range of -3GPa to +3GPa. We assume 2DEG area to be within 0.01$\mu$m range and calculate the 2DEG dose.

Figure 3 shows 2DEG dose vs. stress. As the figure shows for no stress (0GPa) the 2DEG dose is $1.12 \times 10^{13}$/cm$^2$. When a negative stress is applied the 2DEG dose seems to increase with more negative stress and decreases with positive stress. This can be explained by the fact that when we apply negative stress there is some reduction in interface trap charges which enhances the 2DEG dose at the interface. The inverse effect occurs in case of a positive stress.
The I-V characteristics of the proposed device have been shown in figure 4(a). As observed the drain current increases with increasing negative stress and decreases with positive stress compared with no stress condition. This follows the same trend as 2DEG region with respect to different stress conditions. Additionally, we investigated the change in 2DEG and drain current.

The electrical characteristics of the device were investigated for different drain bias voltages and stress conditions. Figure 4(b) shows percentage variation of 2DEG with drain current under stress (positive and negative). We found that percentage change in drain current is approximately half of the 2DEG density change for different bias conditions. Based on these results we are able to establish a linear relationship between drain current and 2DEG for different stress.
Figure 4. The I-V characteristics for no passivation, no stress, positive and negative stress (a) and variation of 2DEG vs. drain current for different drain bias voltages under stress conditions (b).

Figure 5 shows C-V characteristics for different stress conditions for applied gate bias voltage from -5 to +5 V. The increase in interface traps shifts the C-V curve to more negative voltages (13). From the above figure we observe that for +3GPa stress C-V curve shifts towards negative voltage which can be explained as increase in interface traps. But with -3GPa stress C-V shifts towards positive voltage which is accompanied by the decrease in interface traps.

Figure 5. Behavior of C-V with application of gate voltage
Conclusions

In conclusion, we have investigated the influence of different stress condition upon 2DEG region and developed a methodology to find out the linear relation between stress and 2DEG under different stresses and drain bias voltages. The percentage change in 2DEG density for an applied bias and stress condition is twice the percentage change in drain current. C-V characteristics show effect of interface state on 2DEG density and drain current.

Acknowledgments

We are grateful to the National Center, Taiwan in supporting the High-performance Computing for computer time and facilities.

References

5. YUE Yuanzheng, HAO Yue, ZHANG Jincheng, FENG Qian: Journal of Xidian University (2008).
Effect of finger and device-width on ruggedness of nLDMOS device under Single-pulse Unclamped Inductive Switching (UIS) conditions

Neelam Agarwal\textsuperscript{a}, Karuna Nidhi Sharma\textsuperscript{a}, Jung-Ruey Tsai\textsuperscript{a,b,*}, Adarsh B\textsuperscript{a}, Gene Sheu\textsuperscript{a,b} and Shao-Ming Yang\textsuperscript{a}

\textsuperscript{a} Department of Computer Science and Information Engineering, \\
\textsuperscript{b} Department of Photonics and Communication Engineering, \\
Asia University, 500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China. \\
* e-mail: jrtsai@asia.edu.tw

This work demonstrates the effect of increasing finger number and width on the ruggedness of the nLDMOS device under test (DUT). The ruggedness or energy handling capability is analyzed by two-dimensional (2-D) and three dimensional (3-D) device and circuit simulations. The set failure criterion in our study and simulation is the device temperature reaching a critical value equal to the melting point of metal-contacts. The maximum energy is calculated by considering the pass-case prior to device failure and time-integrating the drain voltage and current for the avalanche duration. Maximum avalanche energy handling capability is seen to be increased linearly with number of device fingers. UIS test was also performed on width extended multi-finger nLDMOS device structures. The simulated results provided useful approaches to predict real experimental results and contribute to their physical interpretation by identification of the mechanism of device-failure, hot-spot location and continuous temperature extraction.

\textbf{Introduction}

Inductance is always present to some extent in a practical circuit, and therefore, there is always risk of inducing overvoltage transients when a device with inductive load is switched OFF. Such over-voltage transients may force the device into a state in avalanche where it exceeds its static breakdown voltage (1-4). Device ruggedness is the device’s capability to withstand inductively induced over-voltage spikes. Ruggedness test for device is generally done by subjecting the device to Unclamped Inductive Switching (UIS) stress (1,2). In this brief, we present the observation of the device finger and width effect on Energy in Avalanche, Single pulse (EAS), and prior estimation of Silicon experimental results by simulations. When UIS test is performed on multi-finger devices, higher current level is observed due to increased area and more number of drain terminals. This increased current level leads to higher energy as device finger or width increases.
Device structure and simulation test set-up

The device structure is a lateral diffused n-MOSFET structure with a rated breakdown voltage and threshold voltage of around 42V and 1.2V respectively. Since this device can survive severe UIS stress at high current and voltage levels, it is an ideal candidate for studying the effects of finger and width in avalanche-energy handling capability during unclamped inductive switching. Fig. 1 shows the 2-D cross-sectional view of one nLDMOS cell structure while Fig. 2 shows 2-D cross-sectional view of multi-finger - 4 and 8 fingers, nLDMOS on which UIS test was performed.

Figure 1. 2-D cross-sectional view of one nLDMOS cell structure with geometrical dimensions

Figure 2. 2-D cross-sectional view of multi-finger (4 and 8) nLDMOS with geometrical dimensions, (a) 4-fingers, (b) 8-fingers

Figure 3(a) shows an avalanche-energy capability test circuit or UIS test circuit which was simulated. The simulator solves all the semiconductor equations numerically within the 2-D structure grid using a finite element method. Initially, $E = \frac{1}{2} * L * (I_{\text{peak}})^2$ of energy is stored in the inductor from the drain current flowing when the FET is on (1.5). This energy generates a voltage due to back emf that exceeds the drain-source breakdown voltage when the power is turned off, causing avalanche breakdown in the MOSFET.
Figure 3 (a) UIS test circuit and (b) current and voltage waveforms of the DUT under UIS test conditions

Simulation results and discussion

As shown in the schematic UIS waveform in fig 3(b), the device is pulsed ON for a certain time-period; during this the current ramps up linearly as a function of the supply voltage and the inductor value (L). The device is then turned off and since there is no freewheeling diode to discharge the inductor energy, this energy is forced through the device. Also, once the gate is switched OFF, since the gate voltage is below the threshold voltage, current can’t flow through the channel. The MOSFET enters the avalanche regime and the voltage quickly ramps up to the static breakdown voltage, $BV_{DSS}$. During this time the device breaks down and the current will ramp down linearly as a function of both inductor value (L) and $V_{DD}$ (6).

However, during this time high voltage is seen across the device and high current is being passed through the device. This causes a great deal of self-heating. As can be seen in the waveform, the breakdown voltage rises above the static isothermal level to its effective breakdown level ($V_{BR}$) as the device gets heated up. This is a well known phenomenon due to energy loss to optical phonons and mean free path reduction. As current falls off, the device cools and the breakdown voltage falls back towards its static level. When current ramps down, the drain voltage falls down to supply voltage, $V_{dd}$. Under such scenario, the device is considered to have passed the test for the calculated energy.

Through this test, we intend to find the maximum energy the device can survive at avalanche. Hence, numerous iterations are performed increasing the applied gate-pulse duration ($t_p$) till the device fails due to maximum temperature reached. The set failure criterion in our study and simulation is the instantaneous device temperature reaching a critical value equal to the melting point of metal-contacts (7) which is around 700°C for
Aluminum. Fig. 4 shows the UIS waveforms from simulation for a passed and failed scenario of the DUT.

![UIS waveforms](image)

**Figure 4.** UIS simulated waveforms showing gate voltage, drain voltage and drain current for two cases: (a) Maximum energy handling capability not reached, (b) Avalanche energy exceeds the maximum energy handling capability of the device leading to device failure. Test condition: Vgs = 5V pulse, Vdd=36V, L: 0.16mH for 8-finger device

Maximum energy in avalanche is calculated considering the pass case just before the failure point by time integrating the drain voltage and drain current during avalanche period, i.e, the area in the waveform starting from the point when the gate is OFF till the point once Vdrain reaches VDD(7,8).

When UIS test is performed on multi-finger devices, higher current level is observed due to increased area and more number of drain terminals. This increased current level leads to higher energy \[E = \frac{1}{2} \times L \times (I_{\text{peak}})^2\]. Figure 5 shows maximum avalanche energy the device can handle versus number of device fingers. Energy results for 4, 8 and 12 finger devices from 2-D Medici simulation are plotted in the same scale with the UIS energy results from Silicon experiment done for 300 fingers (listed in Table I). Both simulation and experimental results are for the same inductance value and bias condition. From the above discussion and from plot below, we can infer that Energy handling capability increases linearly with number of device fingers and simulation results can to some extent predict the experimental test results done on Silicon. This can be called as the Finger-effect in avalanche ruggedness of power MOSFETs.
Figure 5. Avalanche energy vs finger number at starting junction temperature of 300K and its extrapolation to the Silicon experimental result

**TABLE I.** Avalanche energy for varied finger numbers at starting junction temperature of 300K.

<table>
<thead>
<tr>
<th>Number of fingers/devices</th>
<th>Maximum Energy taken by the device before failure</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>2.30E-07 J</td>
</tr>
<tr>
<td>8</td>
<td>3.75E-07 J</td>
</tr>
<tr>
<td>12</td>
<td>4.94E-07 J</td>
</tr>
<tr>
<td>300</td>
<td>7.20E-06 J (Silicon experimental data)</td>
</tr>
</tbody>
</table>

We studied the width-effect on maximum energy handling capability of nLDMOS by performing UIS test simulation in Sentaurus 3-D simulator, S-device. UIS test was performed on width extended multi-finger (8 fingers, 16 fingers) nLDMOS device structure of widths - 1µm, 3 µm and 5 µm, extended in Sentaurus device Editor. The DUTs are shown in fig 6.

Figure 6. 3-D visualisation of multi-finger (8 fingers, 16 fingers) nLDMOS device structures having width 1µm, 3 µm and 5 µm each.
The transient plot for maximum device temperature throughout the UIS test for the device pass case and failure case are shown respectively in Figures 7(a) and 7(b) along with gate and drain voltage waveforms. The resulting rise in the maximum device temperature, $T_{\text{max}}$, is seen to be at its peak when the MOSFET is in avalanche regime.

Several iterations are performed between these two cases of device pass and failure to find the maximum $I_{\text{drain}}$ for calculating the device’s EAS capability. Fig 8(a) below shows $I_{\text{drain}}$ at varied gate pulse-width. The incomplete plot of $I_{\text{drain}}$ shows the device failed case since the break-criteria for our UIS test simulation is the point when maximum device temperature reaches 700°C. Hence, the curve immediately prior to the failed case is considered for maximum energy determination.

We know that, energy capability of device for all voltage ranges are completely dominated by thermal effects. Hot-spot locations close to drain terminal can be observed at device failure as shown in figure 8(b). Formation of such hot-spots is seen at the centre of the device due to non-uniform heat dissipation.
Figure 8. (a) Plot of Idrain at varied gate pulse-widths to find $I_{\text{max\_pass}}$ for calculating device’s EAS capability, (b) Temperature distribution at failure showing hot-spot at drain.

Figure 9 shows the plot of calculated maximum avalanche energy the device can handle versus number of fingers and for different widths. For a given inductance and bias condition, energy handling capability is seen to increase almost linearly with width and number of devices. This can be called the width effect in maximum energy handling capability of a device. On plotting the result from Silicon experiment for UIS test done for 300 finger device in the same scale, we can see that Sdevice simulation for EAS capability can predict Silicon experimental measurement results. Table II shows the energy data which are plotted in fig.9.

![Image](image.png)

Figure 9. Avalanche energy vs finger number for device with widths of 1µm, 3 µm and 5 µm each at starting junction temperature of 300K. Energy result for 300 fingers is from Silicon experimental measurement.

<table>
<thead>
<tr>
<th>Number of fingers</th>
<th>Width: 1µm</th>
<th>Width: 3µm</th>
<th>Width: 5µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>5.46E-08 J</td>
<td>5.36E-07 J</td>
<td>1.21E-06 J</td>
</tr>
<tr>
<td>16</td>
<td>1.29E-07 J</td>
<td>7.87E-07 J</td>
<td>1.89E-06 J</td>
</tr>
<tr>
<td>300</td>
<td>7.20E-06 J(Si data)</td>
<td>7.20E-06 J</td>
<td>7.20E-06 J</td>
</tr>
</tbody>
</table>
Conclusions

UIS test is a stress test for MOSFETs to insure that they have adequate avalanche ruggedness for today’s high performance circuits. This work demonstrates the effect of device finger numbers and device-width on the maximum energy handling capability of power MOSFET. Energy handling capability increases linearly with width and number of device fingers. 2-D and 3-D simulation result for avalanche ruggedness of devices, employing this methodology, are found to be in good correlation with Silicon experimental results and hence is a useful approach to predict real experimental results.

Acknowledgments

We are grateful to the National Center, Taiwan for supporting us with the High-performance Computing and facilities. In addition, we would like to thank Vanguard International Semiconductor Corporation, Taiwan for great support and helpful discussion.

References

1. GWS: Unclamped Inductive Switching (UIS) Test and Rating Methodology – AN-2000-000-B
2. Vishay Siliconix, Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments – AN601
6. Application Note: NXP Semiconductors, Power MOSFET single-shot and repetitive avalanche ruggedness rating, Rev. 02 – 27 March 2009, p. 3 of 13
Optimization of nLDMOS Ruggedness under Unclamped Inductive Switching (UIS) Stress Conditions by Poly-gate Extension

Neelam Agarwal\textsuperscript{a}, Karuna Nidhi Sharma\textsuperscript{b}, Jung-Ruey Tsai\textsuperscript{a,b,*}, Gene Sheu\textsuperscript{a,b} and Shao-Ming Yang\textsuperscript{a}

\textsuperscript{a} Department of Computer Science and Information Engineering, 
\textsuperscript{b} Department of Photonics and Communication Engineering, 
Asia University, 500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China. 
\* e-mail: jrtsai@asia.edu.tw

In this paper, the effect of poly-gate extension on improved ruggedness of n-type LDMOS is evaluated by two-dimensional (2D) device and circuit simulation. Multi-finger dimension of n-type LDMOS is subjected to Unclamped Inductive Switching (UIS) stress test to determine its ruggedness. It is shown that the poly-gate extended device yields approximately 15\% higher avalanche energy handling capability (Emax) as compared to that without extended poly-gate region. This work suggests that the improvement in ruggedness of the optimized design is attributed to the suppression and shift of the electric field peaks away from the critical regions. The results from simulation are found to be in good correlation with experimental UIS test results in terms of avalanche energy range, identification of the mechanism of device-failure and hot-spot location. It is believed from the results obtained that this approach will have remarkable impact in the ruggedness if implemented for large-array devices (LAD).

Introduction

nLDMOS devices are common choices as switches in output drivers for inductive loads in industrial and automotive electronic control systems. The switching speed of nLDMOS is so high that at device turn-OFF, inductive load in the circuit can lead to significant over-voltage transients, forcing the device into avalanche and dramatic increase in the device temperature. Under such stressful condition, the device is no longer safe and may lead to device failure. Hence, nLDMOS needs to be designed and manufactured to insure that they have adequate avalanche ruggedness for today’s high performance circuits. Unclamped Inductive Switching (UIS) test is an extremely high stress-test performed on the device under test (DUT) by forcing a charged unclamped inductor to discharge through the DUT (1-3). By UIS methodology, we are able to determine the maximum amount of avalanche energy that can be absorbed by the device prior to its catastrophic failure (4,5). Early LDMOS avalanche reliability tests showed that device failure mainly occurs due to “hot spot” caused by an increase in power dissipation which is a function of local electric field, current density and thermally assisted generation of carriers. If the hot-spot region and peak-electric field can be suppressed in the critical regions of device failure, the device is expected to sustain higher avalanche energy during stress.
In this work, we modify the device structure by extending the poly-gate, as a result of which, suppression of peak-electric field at critical regions of device-failure is seen. To account for the self-heating and temperature rise during the electrical stress, thermodynamic mode is activated. It is also shown that the maximum avalanche energy handling capability of a device is a function of the Starting junction temperature and it decreases as starting temperature increases (1,6). We present the EAS (Energy in Avalanche, Single pulse) for poly-gate extended device compared to original device at starting temperatures from room-temperature 300K (27°C) to 400K (127°C). In all cases, the EAS is found to have improved by the structure-modification.

**UIS Test Simulation Set Up**

Figure 1(a) shows the schematics of UIS test system (1-3) used to test device ruggedness. The UIS waveforms from simulation (1-3,10) are in good agreement with the schematic waveforms shown in Fig 1(b). The device is pulsed ON for a certain time period, during when the current ramps up linearly as a function of the supply voltage and the inductor value (L). During this time, \( E = \frac{1}{2} L (I_{\text{peak}})^2 \) of energy is stored in the inductor from the drain current flowing when the FET is on. The device is then turned off and since there is no freewheeling diode to discharge the stored inductor energy, this energy is forced into the device. The energy appears as an over-voltage spike at the drain. The magnitude of the sudden voltage transient may exceed the rated drain-source breakdown voltage (BV\(_{\text{DSS}}\)) of the device (1,2,7) causing avalanche breakdown in the MOSFET. At avalanche, still higher voltage is seen across the device and high current is being passed through the device which causes a great deal of self-heating. As can be seen in the waveform, the breakdown voltage rises above the static isothermal level (BV\(_{\text{DSS}}\)) to the effective or dynamic breakdown, V\(_{\text{BR}}\), as the device heats up. The gate pulse is turned OFF and hence current starts ramping down. Device cools and the breakdown voltage falls towards its static level. The current will ramp down linearly as a function of both inductance and V\(_{\text{DD}}\) and the drain voltage goes down to supply voltage, VDD (8). Under such scenario, the device is considered to have passed the test for the calculated energy.

Numerous iterations are performed increasing the applied gate-pulse duration (t\(_p\)) till the device fails due to maximum temperature reached. The set failure criterion in our study and simulation is the instantaneous device temperature reaching a critical value equal to the melting point of metal-contacts (5) which is around 700°C for Aluminum. Fig. 2 shows the simulated UIS waveforms for a passed and failed case of the nLDMOS device under test (DUT). The maximum energy in avalanche is calculated considering the pass test-case prior to catastrophic device failure point by time integrating the drain voltage and drain current during avalanche duration (t\(_{\text{AV}}\)) (4-6), i.e., the area in the waveform starting from the point when the gate is OFF till the point once V\(_{\text{drain}}\) reaches V\(_{\text{DD}}\).
Figure 1. (a) UIS test circuit and (b) current and voltage waveforms of the DUT under UIS test conditions.

Figure 2. UIS simulated waveforms showing gate voltage, drain voltage and drain current for two cases: (a) Maximum energy handling capability not reached, (b) Avalanche energy exceeds the maximum energy handling capability of the device leading to device failure. Test condition: $V_{gs} = 5\text{V}$ pulse, $V_{dd}=36\text{V}$, $L: 0.16\text{mH}$ for 8-finger device.
Results and Discussion

Device Structure for test

To understand the modification done in device-structure, the original nLDMOS device structure is first described. Figure 3(a) shows the 2-D cross-sectional view of one nLDMOS cell. The device has a rated breakdown voltage of around 42.3V. Since this device can survive severe UIS stress at high current and voltage levels, it is an ideal candidate for studying the avalanche-energy handling capability during UIS. Figure 3(b) shows 2-D cross-sectional view of multi-finger (8 fingers) nLDMOS DUT. UIS test simulation waveforms shown in Figure 2 above are from the UIS test performed on the device structure shown in Figure 3(b).

![Figure 3](image)

Figure 3. 2-D cross-sectional view of (a) one nLDMOS cell structure, (b) multi-finger [8 fingers] nLDMOS with geometrical dimensions

The device structure with the poly-gate length extended towards the drain terminal by 0.5µm is presented. Figure 4(a) and (b) shows the comparison between the poly-gate length of the original device and modified device structure. Figure 4(c) below shows that Off-state breakdown has increased by 2V for poly-gate length extended structure. However, the threshold voltage and the on-resistance are not affected by a considerable amount.

![Figure 4](image)

Figure 4(a) Original nLDMOS poly-gate, (b) Modified structure with poly-gate length extended by 0.5 µm, (c) Comparison of Off-state breakdown voltage
A critical component for UIS rating is the device’s starting junction temperature. EAS capability of a device is inversely proportional to its starting junction temperature. Maximum energy in avalanche resulting from UIS stress test was examined for both the original and poly-gate modified device structures at starting temperatures from room-temperature 300K (27°C) to 400K (127°C). As shown in Figure 5, avalanche energy raised to the $\frac{3}{4}$ th power is plotted against the starting temperature. The energy values are listed in Table I and II. From the plot, we see that, for a given inductance and bias condition, EAS capability of the device decreases as starting junction temperature increases. Moreover, operating a device at higher junction temperatures reduces the long-term reliability of the device. Table II also shows that Energy handling capability improves by approximately 15% for poly-gate extended device structure.

![Figure 5. (Avalanche Energy)$^{3/4}$ vs Starting junction Temperature (K) for original device and poly-gate extended device. Test condition: $V_{gs} = 5$ V pulse, $V_{dd}=36$ V, $L=0.16$ mH.](image)

**TABLE I.** Energy data for original device – 8 fingers, 1µm width.

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>Imax_pass (A)</th>
<th>(Energy)$^{3/4}$ (J)</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>2.887E-02</td>
<td>1.516E-05</td>
</tr>
<tr>
<td>350</td>
<td>2.807E-02</td>
<td>1.45E-05</td>
</tr>
<tr>
<td>400</td>
<td>2.582E-02</td>
<td>1.32E-05</td>
</tr>
</tbody>
</table>

**TABLE II.** Energy data for poly-gate extended device – 8 fingers, 1µm width.

<table>
<thead>
<tr>
<th>Temperature (K)</th>
<th>Imax_pass (A)</th>
<th>(Energy)$^{3/4}$ (J)</th>
<th>%Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>300</td>
<td>3.121E-02</td>
<td>1.603E-05</td>
<td>7.8%</td>
</tr>
<tr>
<td>350</td>
<td>2.811E-02</td>
<td>1.57E-05</td>
<td>11%</td>
</tr>
<tr>
<td>400</td>
<td>2.535E-02</td>
<td>1.32E-05</td>
<td>22.3%</td>
</tr>
</tbody>
</table>
Electric Field and Temperature Distribution

The improvement in avalanche ruggedness of the modified device is attributed to the reduction in the peak electric-field along the cut-line as shown in Figure 6(a). The plot shows the comparison of electric-field of original and modified device after UIS stress condition with equal stress applied to both devices i.e., maintaining $t_p$ the same.

Cross sections of the device after UIS stress condition show some important phenomena. The temperature profiles in Figures 6(b) and 6(c) show that heating occurs mostly at the vertical p-n junction boundary (Pbody/HVNW). This is where the device breaks down which is expected for a good rugged device design. It is to be noted that the “hot spot” location, which is seen close to the drain terminal (pointed by the arrow) in the original structure, has not yet formed for modified structure under the same applied gate pulse-width (equal stress applied to both devices). Hot-spot is caused by an increase in power dissipation which is a function of local electric field, current density and thermally assisted generation of carriers (9,10). The modified structure shows a lower peak in electric field and lower temperature rise when compared to original structure and hence it is capable of handling more amount of avalanche energy, showing improved RUGGEDNESS.

![Figure 6(a) Comparison of electric field distribution along the cut-line for original and poly-gate extended device, (b) Temperature distribution in original device after UIS stress showing hot-spot at drain, (c) Temperature distribution in modified device structure](image)
Conclusions

In this paper, the effect of poly-gate extension on improved ruggedness of nLDMOS device is evaluated. The simulation results strongly suggest that for the device studied here, poly-gate extension by 0.5µm yields approximately 15% higher energy handling capability (Emax) when compared to original device structure at all temperatures. It is also shown that the maximum avalanche energy handling capability of a device is a function of the Starting junction temperature and it decreases as starting temperature increases.

Acknowledgments

We are grateful to the National Center, Taiwan for supporting us with High-performance computing and facilities. In addition, we would like to thank Vanguard International Semiconductor Corporation, Taiwan for their great support and helpful discussion.

References

1. Vishay Siliconix, Unclamped Inductive Switching Rugged MOSFETs for Rugged Environments – AN601
2. GWS: Unclamped Inductive Switching (UIS) Test and Rating Methodology – AN-2000-000-B
8. Application Note: NXP Semiconductors, Power MOSFET single-shot and repetitive avalanche ruggedness rating, Rev. 02 – 27 March 2009, p. 3 of 13
10. Kevin Fischer and Krishna Shenai, Senior member, IEEE, Electrothermal Effects During Unclamped Inductive Switching (UIS) of Power MOSFET.
Energy Capability of LDMOS as a Function of Ambient Temperature

Adarsh Basavalingappa*, Anumeha, Gene Sheu
Department of Computer Science and Information Engineering, Asia University, 500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan
E-mail: adarsh.b88@gmail.com*

Abstract—Energy capability of a LDMOS device structure is shown to have nonlinear relationship with ambient temperature. Analytical model for energy capability has been discussed and is in good agreement with the simulation results. The dependency of critical temperature on ambient temperature is shown.

Keywords-laterally diffused MOS(LDMOS); critical temperature; thermal failure; energy capability; ambient temperature; SOA; TCAD simulation

I. INTRODUCTION

LDMOS has become the most important member of power semiconductor devices because of its robustness, power capability, cost, reliability, high voltage, high frequency applications, and also because of its superior performance with respect to linearity and efficiency. However device heating under transistor operation results in performance degradation or even thermal runaway. Hence understanding the thermal effects, which is one of the principle failure mechanisms, is very important for designing and optimizing the device to have high energy handling capability.

Safe operating area is a fundamental limiting property of the LDMOS devices as claimed by work of Hower et al. [1], [2]. It was shown by [3] that these devices will be affected by electro-thermal instabilities as both electrical and thermal effects are coupled in nature unlike the claims of [4] where the device will be affected by electrical or thermal instability. Localized heat source concept is considered and analytical model for thermal breakdown has been developed in the past [5]. The major complexity in this method is the strong temperature dependence of the material parameters thermal conductivity (K) and thermal diffusivity (D). Using the appropriate effective values of K and D is very important [6]. Previous works of Hagino et al. [7] and Khemka et al. [8] have assumed constant values for K and D for all the ambient temperature conditions and have concluded that energy capability has a linear dependency over ambient temperature. In this paper the LDMOS energy capability has been studied making use of TCAD software Sentaurus [9] and we see nonlinear relationship between energy capability and ambient temperature. The calculated energy capability values from the proposed analytical model are in good agreement with the simulation results.

II. ANALYTICAL MODELING

An analytical heat flow model is necessary for calculating both electrical and thermal safe operating area. We follow the Green function approach of Dwyer et al. [5]. A thin rectangle of dimension a x b on a semi-infinite silicon surface at z=0 is assumed to represent the heat source. A three-dimensional view of the heat flow region is shown in Fig. 1. Thermal failure of a semi-infinite piece of semiconductor subjected to a rectangular power pulse is assumed to occur when the critical temperature is reached, where the excess carrier generated due to thermal effects exceeds the majority carrier concentration. For a surface heat source of lateral dimensions a x b in a semi-infinite medium (a≥b), power to failure depends on the time scale with respect to the characteristic diffusion times $t_a$, $t_b$ associated to these dimensions, where these times represent the time required for the thermal gradient to reach equilibrium in the dimensions a and b respectively [5] and are given by the following formulae

$$t_a = \frac{a^2}{4\pi D} \quad \text{and} \quad t_b = \frac{b^2}{4\pi D} \quad (1)$$

Where D is the thermal diffusivity (cm²/s).

Since c ≤ a, the device reaches complete thermal equilibrium after a time of approximately $t_c$.

The energy capability of the device E can be calculated in Joules by using the equation

$$E = P_0 X t = \frac{(T_c - T_0)ab\sqrt{\pi K\rho C_p t}}{\int_0^t \tau^2 \text{erf} \left( \frac{a}{4\sqrt{D\tau}} \right) \text{erf} \left( \frac{b}{4\sqrt{D\tau}} \right) d\tau} \quad (2)$$
where $P_0$ is magnitude of the constant pulse power (W), $t$ is the period (s), $T_c$ is the critical temperature (K), $T_0$ is the ambient temperature (K), $\rho$ is the mass density ($g/cm^3$), $C_p$ is the specific heat capacity (J/gK), $K$ is the thermal conductivity (W/cmK), and $D$ is the thermal diffusivity (cm$^2$/s), given by $K/\rho C_p$.

In the previous works [7], [8] the thermal conductivity and thermal diffusivity are assumed to be constant in their calculations but these material constants are highly temperature dependent [10], [11] and should be given appropriate effective values.

A good estimate of energy capability can be obtained by simplifying equations and by using approximations for the error function:

$$\text{erf}\left(\frac{a}{4\sqrt{D t}}\right) \approx \frac{t_a}{t}, \text{ If } t \geq t_a$$

$$\text{erf}\left(\frac{a}{4\sqrt{D t}}\right) \approx 1, \text{ If } t \leq t_a$$

The energy capability can then be written in three different time ranges as

Region I

$$E = \frac{abK\sqrt{\pi t} (T_c - T_0)}{\sqrt{4D}}, 0 \leq t \leq t_b$$

Region II

$$E = 2a\pi K (T_c - T_0) \left[\ln\left(\frac{t_a}{t_b}\right) + 2\right], t_b \leq t \leq t_a$$

Region III

$$E = 2a\pi K (T_c - T_0) \left[\ln\left(\frac{t_a}{t_b}\right) - 2\frac{t_f}{t} + 4\right], t_a \leq t_f$$

The energy capability can then be written in three different time ranges as

The dimension of heat source $a$ and $b$ plays an important role in estimating the energy capability of the device at higher ambient temperatures. So, the thermal expansion was considered to calculate the heat source dimensions at higher ambient temperatures. For the temperature range 293 to 1000 K the linear thermal expansion coefficients $\alpha$ of silicon have been determined by [12]. The values of $\alpha(T)$ were calculated by applying

$$\alpha(T) = \Delta L / (L_0 \Delta T)$$

Where $\Delta T$ is a given temperature change from initial to final temperature, $L_0$ is the initial length of sample at room temperature and $\Delta L$ is the change of sample length from initial to final length of the sample. A fifth order polynomial function of temperature was obtained by the method of least squares:

At 293 $\leq T \leq 1025$,

$$\alpha(T) = -3.0451 \times 10^{-6} (K^{-1}) - 7.981 \times 10^{-5} T^2 + 9.5783 \times 10^{-8} T^3 - 5.8919 \times 10^{-11} T^4 + 1.4614 \times 10^{-14} T^5$$

III. TEST DESCRIPTION

Fig. 2 shows the schematic of cross-section of 800V LDMOS device structure used in this paper. A drain to source voltage pulse ($V_{ds}$) was applied on the DUT and a constant drain current ($I_{ds}$) was maintained for a time long enough to destroy the device. Energy capability of the device was then calculated by integrating the product of $V_{ds}$, $I_{ds}$ along the pulse width ($t$).

The increase of the temperature inside the LDMOS during its operation can degrade the characteristics and
performance of the circuitry, or may even lead to thermal runaway. The temperature rise increases the effective intrinsic carrier concentration inside the device. The device is assumed to fail when the maximum temperature reaches the so-called critical temperature, inducing high leakage current.

IV. RESULTS AND DISCUSSION

The device simulations were performed using thermodynamic and impact ionization models. A typical drain current and temperature waveform is plotted against time for the 300K ambient temperature case in Fig. 3. We can observe a sudden rise in current at 0.5ms leading to thermal runaway. The device fails when the maximum temperature reaches the critical temperature $T_c$. At the critical temperature the leakage current of the device approaches the applied current and gate control is lost [13]. Fig. 4 shows the temperature versus time plot for different ambient temperatures. The time to failure decreases with increasing ambient temperature. A change in critical temperature was observed for different ambient temperatures as shown in Fig. 5. The previous study reports that the critical temperature changes for two different drain to source voltages for a given ambient temperature [8]. As seen from the simulation results the critical temperature increases with increasing ambient temperature for a given drain to source voltage. A linear fit was obtained for critical temperature as a function of ambient temperature given by the equation,

$$T_c = mT_0 + T_{\text{intercept}}$$  \hspace{1cm} (10)

where the slope ‘$m$’ was obtained to be 0.1751 and ‘$T_{\text{intercept}}$’ to be 805.83. Further investigation is required to properly understand and confirm the relationship.

Fig. 6 shows the energy capability of the device versus ambient temperature. Non-linearity of the energy capability as a function of ambient temperature is observed from the simulation as well as analytical solution. A linear dependence between energy capability and ambient temperature was reported earlier in insulated gate bipolar transistors (IGBT) [7] and RESURF LDMOSFETs [8]. High ambient temperature data could have shown the nonlinear property. The model was fit assuming the material constants $K$ and $D$ to be independent of temperature. But in reality these parameters are temperature dependent and should be given appropriate effective values. We made use of appropriate values in our calculations based on the ambient temperature, and also the linear thermal expansion coefficient ($\alpha$) was taken into consideration.
V. CONCLUSION

We have shown that the relationship between energy capability and ambient temperature is nonlinear in nature, and also we have discussed an analytical model to calculate the same. Energy calculated using the proposed analytical models are in good agreement with the simulation results. It is shown that using appropriate values for the thermal conductivity and thermal diffusivity in the calculations is very important. It is also observed that critical temperature of the device increases with the ambient temperature.

ACKNOWLEDGMENT

We are grateful to the National Center for High-performance Computing, Taiwan, for computer time and facilities.

REFERENCES

Triangle Pulse Measurement at Elevated Temperature Novel Measurement for NBTI Assessment

Surya Kris Amethystna1, Karuna Nidhi1, Gene Sheu1,2, Jung-Ruey Tsai1,2, and Shao-Ming Yang1,
1Department of Computer Science and Information Engineering, Asia University, 2Department of Photonics and Communication Engineering, Asia University 500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China Email: jrtsai@asia.edu.tw

Abstract—This paper proposed a triangle pulse measurement with elevated temperature to assess the existence of hydrogen in the Si-SiO2 interface. Silicon-Hydrogen bond in Si-SiO2 interface is responsible to increasing of absolute device threshold voltage due to negative bias temperature instability on p-channel transistor. Reaction-Diffusion as the most commonly accepted model for negative bias temperature instability interpret the interface trap generation during negative bias temperature stress by phenomenon of broken Si-H bonds at Si-SiO2 interface (reaction) and hydrogen removal (diffusion). Temperature stress can accelerate Si-H bond dissociation (reaction phase) and give a better assessment of initial creation of interface trap generation which is correspond to the concentration of hydrogen in the Si-SiO2 interface. 100ns pulse rising and falling time is used as threshold voltage measurement to eliminate the NBTI recovery effect.

Keywords-component; NBTI; R-D model; Temperature; Pulse Measurement

I. INTRODUCTION (HEADING 1)

Nowadays, negative bias temperature instability (NBTI) has reintroduced as a major reliability concern for mainstream analog and digital circuit due to processing and scaling changes integrated circuit process technology [1-3]. Degradation of drain saturation current and increase of absolute threshold voltage in p-channel transistor leads to significant timing issues and reduction of standard random access memory noise margin respectively [4]. Another technological factor along with other specific usages, have made NBTI as one of the foremost reliability concern for modern integrated circuit (almost as important as gate oxide time dependent dielectric breakdown reliability) [5].

During integrated circuit fabrication such as nitride deposition and forming gas annealing, hydrogen is the most common impurity which being incorporated into the oxide and distributed non-uniformly with concentration found pileup near the Si-SiO2 interface. Transistor may contain high or low hydrogen concentration depends on its process and annealing condition. Hydrogen itself is believed to be the main passivating species for silicon dangling bonds and plays an important role during NBTI stress [4].

Jeppson and Svenson were first proposed a model for negative bias temperature instability [6]. Hydrogen from Silicon-Hydrogen electrically activated to form an interface trap. Interface traps are electrically active defect with an energy distribution throughout the silicon band gap. Since electrons and holes occupy interface traps, they become charged and contribute to threshold voltage shift, given by

\[ \Delta V_T = - \frac{\Delta q N_{IT}(\Phi)}{C_{ox}} \] (1)

In p-channel transistors interface traps are positively charged, generated donor type interface traps and leading to negative threshold voltage [7].

Reaction-Diffusion model can interpret the power law dependence of interface trap generation during NBTI [5]. When gate biased at particular voltage, it initiates a field-dependent reaction at Si-SiO2 interface which break the passivated Si-H bond and generates an interface traps. Initial interface trap generation rate depends on reaction phase (Si-H bond dissociation) and later rate depends on diffusion phase (hydrogen diffuse in the oxide). Temperature stress will affect to weaken energy of Si-H bond so that increases the number of generated interface traps.

This study proposed a pulse measurement technique with elevated temperature instead of electric field stress to assess the hydrogen incorporated in Si-SiO2 interface. Since there is no field dependent on diffusing species which means it is assumed neutral [5], we put more attention on reaction part of R-D model. Indeed, it was a critical point when Si-H bond broken and only limited by the number of hydrogen concentration which able to react. Elevated temperature is used to weaken and broke the as many Si-H bonds as possible to create initial interface trap generation. Threshold voltage shift which is corresponding to the number of generated interface trap then measured using a rising and falling time of triangle shape pulse to minimize recovery effect.

II. EXPERIMENTAL SETUP

This study was done using standard PMOS 0.25um 5V BCD technology.
Setup of experiment was shown in Figure 1 and 2 (a) (b). Conventional direct current current-voltage (DCIV) was first employed without any elevated temperature. Device was stress at a room temperature (300K) with constant 5MV/cm negative electric field across the gate oxide while source, drain and substrate were grounded.

This DC measurement is used to see the activation of Si-H bond generating interface traps by influence of electric field stress. Varying electric field stresses (2.5, 5, and 7.5MV/cm) and elevated temperature (300K and 350K) then employed to analyze its behavior. Threshold voltage shift calculated start form 0.5 second stress until 10 hours as maximum applied stress time and plot a degradation trend line.

Second experiment involves a triangle pulse as a measurement technique with an elevated temperature as seen on Figure 2 (a). Device treated at three different temperatures (300K-350K-400K) with drain voltage maintain 0.1V and grounded source-substrate contact. Triangle shape pulse with 100ns rising and falling time then biased to gate in order to measure \( I_d-V_g \). Pulse rising time proposed as a initial \( I_d-V_g \) while pulse falling time proposed as degraded \( I_d-V_g \) as seen on Figure 2 (b).

### III. RESULT AND DISCUSSION

We divide our study into two part. First part was mainly used to understand the interface traps generation behavior due to negative bias temperature instability on p-channel transistor and second one was our proposed measurement technique.

A. Direct Current Current-Voltage (DCIV)

Degradation trend for conventional DCIV in Figure 3 give us information that after 10 hours stress time, device absolute threshold voltage shifts 2% higher from its original value. It also found that threshold voltage shift percentage was jumping up and down at a stress time shorter than 6 minutes (0.1 hours). That phenomenon can be explained by NBTI recovery effect. Interface traps generated at a previous stress reduced and result a lower threshold voltage shift for next stress. However, this effect becomes less significant as a long stress time applied.

We also successfully simulating threshold voltage degradation trend using TCAD Sentaurus simulator. Simulation result has a good agreement against the silicon data as seen on Figure 3.
Figure 5. Behaviour of generated interface trap by influence of electric field and temperature stress.

Figure 4 shows generated interface trap evolution as a function of stress time as well as its distribution at Si-SiO$_2$ interface due to DCIV stress at room temperature. Maximum interface traps measured after 10 hours stress is around 3e10. It was distributed uniformly under entire the gate region. That number was responsible to 2% device threshold voltage shift.

From the experiment in Figure 5, we also found that temperature stress play a significant role in the initial Nit generation rather than electric field stress. Increasing electric field stress (2.5 – 7.5MV/cm) at the device, does not make a serious different on initial Nit generation. But, different result occurs when elevated temperature stress applied. Elevate the temperature to 350K can increase initial Nit generation even at low electric field stress. It proves that temperature stress profoundly efficient to break Si-H bond and create Nit compare to electric field stress.

B. Fast Pulse Measurement With Elevated Temperature

DCIV measurement technique at room temperature suffers NBTI recovery and become a major limitation to understand NBTI mechanism. As a result, it will underestimate the total number of interface traps (Nit). We develop a triangle pulse with 100ns rising and falling time as a measurement unit to overcome such a recovery effect problem. Those pulse rising and falling time was fast enough to be considered as a free NBTI recovery measurement [9].

We have done an experiment with three different temperatures. First experiment was done in room temperature, second and third done at 350K And 400K respectively. As mention earlier, elevated temperature absolutely needed in order to break as many Si-H bonds as possible. When pulse on Figure 2 (b) applied, device will show current-voltage response as seen on Figure 6. Threshold voltage shift from rising and falling time can be explained by the difference of initial generated interface trap. The number then extracted as plotted on Figure 7 for every measured temperature. We take a normalization line at 300K, assume that there is no interface trap generated during the measurement. When stress temperature increase to 350K, its found 2.98mV threshold voltage degradation. According to the relationships between $\Delta V_{th}$ and $\Delta N_t$ from (1) on introduction section, that degradation is contributed by creation of ~5e11 interface traps.

Same phenomenon happened when stress temperature set to 400K. Threshold voltage shift 3.46mV which contributed by creation of ~6e11 interface traps.

We develop a worst case scenario in this study. This means we provide unlimited Si-H bond that can be broken and generates initial interface trap on the reaction phase of Reaction-Diffusion Model while, in the actual case it will limited by availability of hydrogen in Si-H bonds. Degradation trend line on Figure 7 shows that 350K–400K seems to be most suitable temperature stress applied since there will be no significant increase on initial Nit generation if stress temperature goes beyond 400K.

In actual case, excessive shift caused by this novel measurement technique indicates that such fabrication process contains a lot of hydrogen contamination and finally resulted NBTI prone device.

IV. CONCLUSION

This paper was successfully develop and simulates a novel measurement technique to characterize NBTI more accurately by evaluating the number of hydrogen at Si-SiO$_2$ interface. Temperature stress and fast triangle pulse with 100ns rise and
fall time has proven to be more efficient to distinguish which device has more hydrogen contaminated.

Acknowledgment

The authors would like to thank Vanguard International Semiconductor Corp. for their useful support and discussion

REFERENCES

ti and HCI,” IRW Final Report, 2000
Interface Trap Mapping for HCI Reliability Assessment on Bend Gate Structure

Brilliant Adhi Prabowo1, Surya Kris Amethystna1, Gene Sheu1,2, Jung-Ruey Tsai1,2*, and Shao-Ming Yang1,
1Department of Computer Science and Information Engineering, Asia University,
2Department of Photonics and Communication Engineering, Asia University
500, Lioufeng Rd., Wufeng, Taichung 41354, Taiwan, Republic of China
Email: jrtsai@asia.edu.tw *

Abstract—This paper demonstrates mechanism of interface trap generation and the device degradation evaluations due to hot carrier injection stress for a various gate structure by TCAD simulation. In this study, Fowler-Nordheim Tunneling, Lucky Electron Injection, and Thermionic (HCI) model were employed to perform accurate physics phenomenon during hot carrier stress test. This three dimensional (3D) device structure simulation gives not only the number of interface trap (N_{IT}) but also its distribution on the Si/SiO_{2} interface. Interface trap generated for three type of gate structures were evaluated and bend gate structure is suffer a higher generated interface trap after hot carrier stress compare to stripe gate structure which leads to worse R_{ON} and I_{dsat} degradation.

Keywords: Hot Carrier Injection; Interface Trap; Bend Gate; TCAD; 3D Simulation

I. INTRODUCTION

Nowadays, on power amplifier and drivers applications, multi-finger MOSFET structure plays a very important roles because of its advantages, such as the capability to drive a larger current, and able to reduce the snapback voltage during ESD testing for power device application[1]. Due to increasing the large number of finger and to get effective packing density with the total limited large array devices (LAD) area, the non-rectangular and bend gate design on MOSFET were proposed and investigated [2,3]. The main obstacle of the MOSFET with bend gate structure is the drain current degradation caused shorter device lifetime due to hot carrier injection, but the mechanism of this reliability issue was not well understood [3].

High kinetic energy of carriers is gained under the influence of high lateral fields in MOSFET channel and pinch-off region of the transistor. Hot carrier will be generated when non-equilibrium energy distribution is reached and impact ionization will be triggered. Sufficient energy, approximately 3.6 eV for electrons and 5.0 eV for holes in silicon, can be acquired by hot carriers to surmount the energy barrier at Si/SiO_{2} interface or tunnel into the oxide and the defect will be raised when injected carriers interact with the oxide. This instability may appears and cause a device parameter shift in a long term operation of the device. [3-5].

In order to make an assessment of device reliability, hot carrier injection stress should be performed and followed by charge pumping measurement to evaluate the interface trap density for the degraded device. The influence of hot carrier injection on the performance of MOSFET has been studied extensively. As the shrinking of device geometry, the degradation effect will be more significantly influence the devices reliability. It was reported for n-channel transistors, the interface traps generation by impact-ionization carrier is the most influence factor for the hot carrier degradation [4,6].

In this study, the first 3D TCAD simulation analysis of interface traps generation due to HCI on bend gate structure is presented. Three different structures were investigated, conventional stripe gate structure, and bend gate structures with different bending length of poly-silicon as shown in fig. 1(a,b,c) respectively. The 3D electrical characteristics are reported, such as top view mapping of Si/SiO_{2} interface, the number of generated interface traps (N_{IT}) and its distribution.

II. EXPERIMENTAL SETUP

Standard 0.25μm 5V BCD NMOS process simulation using TCAD-Sentaurus Sprocess was employed in this study. The device structure has 125 Å of gate oxide thickness, and 0.2 μm of a poly-silicon gate thickness, the only difference on these structures is poly-silicon design in order minimize the number of contacts. Special mask was needed to create 45° of a bend gate angle as shown on fig. 1 (b) and (c). For multi-finger structure, the smallest area LAD in this research was occupied by bend gate design structure with bending length (l) gate of a 0.103 μm as shown on fig. 1(c).

Figure 1. Structure comparison (a) Structure of Case 1 stripe gate (b) Structure of Case 2 bend gate length 0.075 μm (c) Structure of Case 3 bend gate length 0.103 μm
TCAD Sentaurus Sdevice module was used to simulate its electrical and physical parameter such as breakdown voltage, electric field, impact ionization, linear and saturation drain current and $N_{IT}$ after the sample were simulated under the hot carrier stress for certain time.

The experimental setup was designed as flowchart in fig.2. Practically, the comparisons of the device degradation are performed by confrontation of IV curve before and after stress time on the device structures. Thus, degradation trend for on state resistance ($R_{ON}$) and drain current saturation ($I_{DSAT}$) were calculated for three different stress time (100s, 1000s, and 5000s). Ron were calculated at drain and gate voltage equals to 0.1V and 5V respectively while drain current saturation calculated at 5V of drain and gate voltage respectively. The interface trap generation was monitored during HCI stress simulation.

NMOS device performance is biased to a particular stress condition corresponding to actual hot carrier injection stress. Drain voltage of 5V and gate voltage of 4.5V was used as stress condition. Transient simulation was simulating the stress time for until 5000 seconds. Degradation interface physics model was used to the material interface specification to simulate physical behavior of interface Si/SiO₂ accurately [7].

Thermionic HCI and classical lucky electron model were invoked in the device simulation to perform the interface trap generation due to HCI. A process of electrons tunnel through a barrier in the presence of a high electric field was taken into account by using Fowler-Nordheim model. This quantum mechanical tunneling process is an important mechanism for thin barriers as those in metal-semiconductor junctions on highly-doped semiconductors. While, the lucky-electron model provides an estimate of the probability that a carrier in silicon will be transmitted to the oxide by overcoming the local energy barrier at the Si-SiO₂ interface [8-11].

III. RESULT AND DISCUSSION

Breakdown voltage was performed as the beginning of this study as shown on fig. 3, for longer bend gate structure the lower breakdown voltage were exhibited in comparison to stripe gate which perform 9.38 V. Breakdown voltage were measured of 8.48V and 7.75V for bending length 0.075 µm and 0.103 µm respectively. This phenomenon was investigated by 3D mapping of electric field when breakdown occurs. As shown on fig. 4, the uniform electric field distribution under the striped gate edge on the drain side was occurred, while non-uniform electric field distributions were appeared under bend gate structures. Higher electric field happened under the gate near the drain side area following the gate path. But, highest point is located on the bending area where the maximum impact ionization location supposed to be. Non-uniform electric field is responsible for low breakdown voltage measurement. Because the device fails at bending corner while other area still sustains at that given voltage. Indeed, soft breakdown occurs on the bend gate length 0.103 µm, which gives an explanation that gate corner becomes the weakest point of the device since current crowded occurs there. Thus, we are not includes this structure for the next assessment since its breakdown voltage fall beyond 10% compare to conventional gate.

The initial $N_{IT}$ concentration is assumed 1e10/cm², which means fresh sample itself contain 1e10 interface traps per centimeter square for both first and second case. Simulation result in fig. 5 shows a total interface trap generated during hot carrier stress in the function of stress time. For first case, total interface trap concentration increase up to 6.13e10 traps/cm² just after 0.2 second stress applied to the device and continues increasing until 8.11e11 traps/cm² after 5000 second. Higher generated $N_{IT}$ happened on second case, number of interface trap increase up to 8.52e10 traps/cm² and 8.17e11 traps/cm² after 0.2 second and 5000 second respectively.

Figure 3. Structure comparison (a) Case 1 stripe gate (b) Case 2 bend gate (c) Case 3 bend gate structure

Figure 2. Flowchart of experiments design
Figure 4. Electric field distribution when breakdown occurs on (a) Structure of Case 1 stripe gate (b) Case 2 bend gate length 0.075 µm (c) Case 3 bend gate length 0.103 µm

Figure 5. Total interface trap generation during hot carrier stress

As shown on fig. 5, bend gate structure exhibit higher number of interface trap, the difference of total interface trap is 30% at 0.2 second stress. Meanwhile, when long stress time applied for both cases, the number of total interface trap will reach its saturation point in a reasonable number, slightly below 1e12 traps/cm².

Through this simulation results on fig. 6(c) and 7(c), the distribution of interface trap were investigated. By disclose the visibility of poly silicon, nitride spacer, and oxide, the distribution map of interface trap on the silicon surface will appears. After 5000 seconds stress, the increasing of interface trap occurs under the gate and mainly concentrated at the drain side area. The number increases around 1e11 traps/cm² under the gate area, ten times higher than initial. The evolution of generated interface traps during HCI stress was captured from fig. 6 and 7 [12].

Figure 6. Increasing of interface trap due to HCI stress on stripe gate structure (a) 100s stress (b) 1000s stress (c) 5000s stress

Figure 7. Evolution of interface trap due to HCI stress on bend gate 0.075 µm structure (a) 100s stress (b) 1000s stress (c) 5000s stress

Degradation trend of $R_{ON}$ and drain current saturation were extracted by comparing section number 4 and 6 from fig. 2 for every stress time applied. Figure 8 shows the degradation trend of $R_{ON}$. Bend gate structure exhibit worse performance of hot carrier reliability compare to stripe gate structure. On state resistance of stripe gate structure was degrade 0.44% after 100 second hot carrier injection stress applied while the bend gate structure degrade 0.78%. When the longer stress time applied to the device (5000 seconds) $R_{ON}$ was degraded 0.96% and 1.44% for stripe and bend gate structure respectively.
In addition, similar trend occurs on drain current saturation degradation trends. Drain current saturation of stripe gate degrade 0.89% after 100 second hot carrier injection stress while the bend gate structure degrade 0.98%. Thus, at a longer stress time (5000 seconds) drain current saturation will degrade 1.84% and 2.00% for both stripe gate and bend gate structure.

For on state resistance degradation trend, bend gate structure degrades 50% more after 5000 seconds hot carrier injection stress performed compare to stripe gate structure. For drain current saturation degradation, it degrades 8.7% more.

IV. CONCLUSION

Hot carrier reliability of bend gate structure were simulated and investigated successfully. The increasing of interface traps due to hot carrier injection stress happened under the gate and mainly concentrated on the drain side area. It’s found that bend gate structure has a worse performance of hot carrier injection test compare to stripe gate structure due to current crowded at the bending area. We proposed this method as a test consideration also when the designer want to create a bend gate structure for logic or large array device.

ACKNOWLEDGMENT

The authors are grateful to Vanguard International Semiconductor corp. for the valuable discussion on this topic and the National Center, Taiwan for supporting the TCAD licenses to this study.

REFERENCES

Overlapping Pulse Time-Induced Latch-up Investigations in Bootstrapping Technique

Purwadi\textsuperscript{1}, Shu-Ming Bai\textsuperscript{1}, Jung-Ruey Tsai\textsuperscript{2*}, Shao-Ming Yang\textsuperscript{1}, Gene Sheu\textsuperscript{1}
\textsuperscript{1}Department of Computer Science and Information Engineering, Asia University
\textsuperscript{2}Department of Photonics and Communications Engineering, Asia University
500, Liofeng Rd, Taichung 41354, China
Email: jrtsai@asia.edu.tw

Abstract- Latch-Up occurrence of the complementary metal oxide semiconductor (CMOS) inverter applied in bootstrapping driver circuit are presented by 2 dimensional device simulations. The overlapping pulse time could trigger on the parasitic silicon control rectifier (SCR) inside the CMOS, shown by currents crowding plot. The curve overlap versus rise time are plotted to divide the free latch up design area and latch up area.

Keywords-component; Latch-up; CMOS inverter; overlapping pulse time

I. INTRODUCTION

CMOS technology widely applied in such as Radio Frequency (RF), System on Chip (SoC), Mixed Signal, and Power Supply etc. With aggressive of scaling the CMOS, this device will susceptible on latch up occurrence. In previous study, several trigger mechanism have been proven to be a source of latch up occurrence [1-6]. Most of paper published talk about the latch up that is stimulated by ESD [4-6]. This paper will present another stimulation of latch up in case of overlapping pulses time in bootstrapping technique.

The low voltage and low power CMOS inverter circuit is widespread used as driver using bootstrapping technique. This bootstrapping technique is desired to improve the power dissipation, higher speed, and reduction active area [8]. This technique uses a capacitor to couple to the voltage of the source. It produces an output voltage higher than the source voltage. In an indirect bootstrap [9], fig.1, increasing the voltage used to maintain the gate voltage of high NMOS Q1 always above the source voltage.

![Bootstrapping circuit with capacitor Cbst](image1)

Figure 1. Bootstrapping circuit with capacitor Cbst

![HS floating driver](image2)

Figure 2. HS floating driver that is built by many CMOS logic arranged in parallel and PWR Stage

CMOS devices in the circuit power (PWR) stage and High Side (HS) Floating Diver fig.2, will have a different voltage at each node BST, DRVH, and SW illustrated by timing diagram in fig.3 and fig. 4. Programmable delay is needed to keep the timing diagrams are not overlapping [10]. This paper describes the effect of the overlapping time in CMOS inverter device, which can trigger on the CMOS inverter parasitic SCR. To investigate it, the timing diagram pulse is applied to the test structure with several variations of overlapping time.

![Non Overlap Timing Diagram](image3)

Figure 3. Non Overlap Timing Diagram
II. EXPERIMENTAL METHODOLOGY

Bootstrap circuit, fig.1, consists of VDD, and bootstrap capacitor (Cbst). When the system starts working the SW pin is at 0 volt condition, so Cbst in charge until it reaches VDD. When the Pulse Width Modulations (PWM) logic turns into a high, floating HS drivers will begin to turn on and it will also turn on the High Side MOSFET, Q1, by encouraging Cbst. When Q1 is on, the voltage at the SW will rise up to VIN, and will encourage the BST pin to VIN + VCBST voltage level, and DRVH will become VIN+VCbst which is enough for the gate to source voltage to hold Q1 stays on. To complete a cycle, Q1 is switched off by lowering the SW pin voltage. When the low side MOSFET, Q2, turn ON, the SW pin scaled to 0 volt. With so Cbst will discharge again until VDD, to be repeated in subsequent cycles. So, the voltage condition on BST, DRVH and SW pin can be mapped as shown in fig.2 [10].

HS floating Driver built by many CMOS inverter arranged in parallel. To simulate the effect of overlapping pulses, one device is taken as a sample. The samples used were 5V CMOS 0.25um technology. Lay out of the device shown in fig.5. The device under test (DUT) is established using TSuprem-IV software. Then, device simulation is done using Medici.

With the Medici ability to establish pulses in fig.3 and fig.4, the TLU caused by overlapping can be simulated. Then, both of the timing diagrams are applied to single device of CMOS inverter. Simulation is done in time domain using the transient analysis solution. CONMOB model is used to solve the concentration dependent mobility. The long silicon and silicon trench insulator (STI) interface between PMOS and NMOS may have effect on carrier mobility due to surface scattering. Then, a surface mobility is specified with SRFMOB. Impact

III. RESULT

Latch up occurrence was not found in non overlapping time. Then, we make the SW overlap and increase the overlapping time until the device latch-up. We find the critical overlapping time value. The device does not latch up when the overlapping time less than 3 nanoseconds and the device latch up at overlapping time more than 4 nanoseconds for rise time 10 ns. Figure 6 (b) shows no current flow in the substrate when the device works at the non overlapping time or in some tolerance of overlapping time.

Figure 6 (a) shows the current level in the non overlap and 3ns overlap are in hundreds microampere. Compare to both non and 3 ns overlap, the 4 ns overlapping have huge current shown fig.7 (a), that is in hundreds miliampere current level. The huge current trough the substrate means that parasitic SCR has triggered on, so latch up is occurred. Huge current in the substrate shown in fig.7 (b).

In this experiment we vary the values of overlapping time and rise time. From a combination of both overlapping and rise time, we create curve that divides the latch up areas and
free latch up areas. This curve can be used to determine how sensitive programmable delay that must be provided to prevent the latch up occurrence.

I. DISCUSSION

Figure 5 shows typical circuit structure and device cross-sectional view of the CMOS inverter. In the CMOS inverter formed PNPN (P+/N-Well/P-well/N+) structure between BST and SW of the CMOS circuit. Equivalent circuit of the SCR is formed by a vertical PNP bipolar junction transistor (BJT) \( Q_{\text{PNP}} \) paired with a NPN BJT \( Q_{\text{NPN}} \). When one of parasitic BJT turn on, a positive feedback mechanism of regeneration within the structure will be initiated. If the beta product of two BJT gain can be maintained more than 1, then latch up will not happen. When the parasitic SCR in CMOS ICs triggered on the latch up will occur. Latch up creates low impedance between BST and SW will be very small, so a big current will flow through the substrate.

The circuit equivalent inside the CMOS inverter device is demonstrated in fig.8 (a), we can identify how the latch-up occurs. To investigate it, we make lines \( t_1, t_2, t_3, \) and \( t_4 \) in fig.8 (b) which shows voltage levels BST, DRVH and SW at the same time. At the time \( t_1 \), the VBST is VDD and SW is 0. In this \( t_1 \), both BJT \( Q_{\text{NPN}} \) and \( Q_{\text{PNP}} \) are not triggered on. At the time \( t_2 \), that is (VSW-VBST)> build in of 2 diode (diode built by the N-channel of drain NMOS and P channel of source PMOS), the current will flow to the BST through DRVH line that indicated by arrows in fig.8 (a). In this condition \( Q_{\text{PNP}} \) will trigger on that will be followed by \( Q_{\text{NPN}} \) which create small impedance in the substrate. Furthermore, at \( t_3 \) the VBST grows rapidly exceeds the VSW. Because \( Q_{\text{PNP}} \) and \( Q_{\text{NPN}} \) are...
triggered on, the current will flow from the BST through the substrate to the SW, shown by the strip line in fig.8 (a). At the time t4, VBST returns to the condition of VDD and SW to 0 volt conditions. In this time, the large currents still flow through the substrate because of latch up occurrence. fig.6 (b) shows the flow of large current after latch-up occurred.

II. CONCLUSIONS

The Latch-up occurrence in the CMOS inverter caused by overlapping time diagram in the bootstrapping technique has been successfully indentified using 2 dimensional simulations Medici. This Latch-up occurrence also has been explained using circuitry analysis. Finally, the curve overlap versus rise time is established that can help bootstrapping designer to make the time diagram.

REFERENCES


A 2-D Analytical Model of SOI High Voltage Devices with Dual Conduction Layers
Tingting Hua¹, Yufeng Guo¹, Ying Yu¹, Xiaojuan Xia¹, Changchun Zhang¹, Gene Sheu²

Abstract—By solving 2-D Poisson’s equation, a new analytical model to calculate the electric field distribution of a SOI RESURF device with Dual Conduction Layers (Dual-CL) is firstly proposed. The proposed model is also available for the single RESURF and triple RESURF SOI devices without any modification. A matrix equation is developed for the determination of the lateral and vertical breakdown voltages, in which the influences of the N-top layer, P-top layer and the N-drift region are all considered. A unified RESURF criterion of single RESURF, triple RESURF and Dual-CL SOI devices is further derived for optimizing the structure parameters. A good agreement between the analytical results and the numerical results shows that the N-top layer and P-top layer have opposite impacts on the breakdown performance of Dual-CL SOI devices. In addition, an optimal trade-off between the breakdown voltage and the specific on-resistance for the triple RESURF and Dual-CL SOI devices is obtained due to the incorporation of the P-top layer.

Keywords—SOI, RESURF, dual conduction layers, model

I. INTRODUCTION
RESURF (Reduced Surface Field) technology is one of the most used methods to design SOI high voltage devices. To suffer high voltage, the doping concentration of the drift region must be low enough so that the drift region can be fully depleted in a RESURF device. As a result, a high specific on-resistance is brought. To overcome such a drawback, many novel device structures have been proposed. The dual conduction layer (Dual-CL) device is one of the effective solutions developed in recent years. In this device, a heavily doped homo-type layer and a buried anti-type layer have been introduced in the drift region. In the on-state operating condition, the device has two parallel conduction paths along the drift region, one above and one below the buried layer, which brings a reduced specific on-resistance. On the other hand, when the device is biased on off-state, the drift region, including the heavily doped homo-type layer, buried anti-type layer and underneath body region, is full-depleted, which means a high breakdown voltage. Although a lot of researches have been done on numerical simulations and experimental fabrications for the device, none of any analytical approaches has been reported to explore the physic mechanism and quantify the operating performance.

A 2-D analytical model of SOI high voltage devices with Dual-CL structure is developed in this paper. It allows for quick and easy calculation of the electric field profiles and the breakdown voltage. It is also available for single and triple RESURF devices. All analytical results of the proposed model are verified by the numerical results simulated by semiconductor device simulator Medici. The paper is organized as follows. The next section describes the derivation of the 2-D analytical model for the potential and electric field distributions in detail. Section 3 investigates the breakdown voltage. Section 4 deals with the RESURF criterion for the optimization of the device parameters. Section 5 shows some examples of using the proposed model, checking also its validity by Medici. Some conclusions are given in section 6.

II. CALCULATION OF THE ELECTRIC FIELD
A cross-section of a Dual-CL SOI LDMOS is shown in Fig. 1, where x measures the horizontal position relative to the left edge of the drift region and y measures the vertical position relative to the surface of the drift region. The n-type drift region has a uniform doping concentration N_d. L is the drift region length. t_s and t_ox are the top silicon thickness and the buried oxide thickness with permittivity of \( \varepsilon_s \) and \( \varepsilon_{ox} \), respectively. The donor and acceptor concentrations implanted in the drift region to form the surfaced n-type (called N-top) layer and buried p-type (called P-top) layer are \( N_{top} \) and \( P_{top} \), respectively. Therefore, the net doping concentrations of the N-top and P-top layers are \( N_{top} + N_{ox} \) and \( N_d - P_{top} \), respectively. The P-top layer is defined by \( x = L_1 \) and \( x = L_2 \) in the lateral direction, and \( y = t_s \) and \( y = t_z \) in the vertical direction. Along the left and right edges of the P-top layer, the whole drift region is divided into region-1, region-2 and region-3. The region-2 is divided into layer-I, layer-II and layer-III along the top and bottom edge lines of the P-top layer. To simplify modeling, the region-2 is investigated at first, then the region-1 and region-3 are treated as the special cases of the region-2 when \( N_{top} = P_{top} = 0 \).

Tingting Hua, Yufeng Guo, Ying Yu, Xiaojuan Xia, and Changchun Zhang are with the College of Electronic Science and Engineering, Nanjing University of Posts and Telecommunications, Nanjing, Jiangsu 210003, China(Tel.: +86 25 862 88235; fax: +86 25 83492322; e-mail: yfguo@njupt.edu.cn).
Gene Sheu is with the Department of Computer Science & Information Engineering, Asia University, Taichung 41354, Taiwan.
The potential function \( \phi_j(x, y) \) can be approximated by two-order Taylor expanded formula of

\[
\phi_{2j}(x, y) = \phi_{2j}(x_0, y_0) + \frac{\partial \phi_{2j}(x_0, y_0)}{\partial x} (x - x_0) + \frac{\partial ^2 \phi_{2j}(x_0, y_0)}{\partial x^2} (x - x_0)^2
\]

where (2) assumes that the vertical electric field at the drain is biased to a positive high voltage \( V_d \), the drift region is full depleted. The electrostatic potentials \( \phi_{2j}(x, y) \) in layer-I, layer-II and layer-III satisfy the 2-D Poisson’s equation

\[
\frac{\partial ^2 \phi_{2j}(x, y)}{\partial x^2} + \frac{\partial ^2 \phi_{2j}(x, y)}{\partial y^2} = -\frac{q N_{2j}}{\varepsilon}, \quad j = I, II, III
\]

where \( N_{2j} = N_{D} + N_{ox} \), \( N_{2II} = N_{D} - P_{ox} \), \( N_{2III} = N_{D} \).

The boundary conditions are given by

\[
\frac{\partial \phi_{2j}(x, y)}{\partial y} \bigg|_{y=0} = 0
\]

\[
\frac{\partial \phi_{2II}(x, y)}{\partial y} \bigg|_{y=y_{ox}} = -\frac{\phi_{2III}(x, t)}{(\varepsilon D_{top})_{t=0}}
\]

\[
\phi_{2j}(x_{t}, t) = \phi_{2II}(x_{t}, t), \quad \frac{\partial \phi_{2j}(x, y)}{\partial y} \bigg|_{y=y_{ox}} = \frac{\partial \phi_{2II}(x, y)}{\partial y} \bigg|_{y=y_{ox}}
\]

\[
\phi_{2j}(L_{j}, 0) = V_d, \quad \phi_{2j}(L_{j}, 0) = V_d
\]

where (7) assumes that the vertical electric field at the semiconductor surface may be minimized \(^{11}\). (3) is the continuity of electric flux density across the Si/SiO\(_2\) interface \(^{12}\). (4)-(5) are the continuity conditions of the potential and electric field along the boundaries of layer-I/layer-II and layer-II/layer-III, respectively. (6) is the surface potentials at the left and right edges of the region-2.

The potential function \( \phi_{2j}(x, y) \) can be approximated by two-order Taylor expanded formula of

\[
\phi_{2j}(x, y) = \phi_{2j}(x_0, y_0) + \frac{\partial \phi_{2j}(x_0, y_0)}{\partial x} (x - x_0) + \frac{\partial ^2 \phi_{2j}(x_0, y_0)}{\partial x^2} (x - x_0)^2
\]

\[
\phi_{2j}(x, y) = \phi_{2j}(x_{t}, t) + \frac{\partial \phi_{2j}(x_{t}, t)}{\partial x} (x - x_{t}) + \frac{\partial ^2 \phi_{2j}(x_{t}, t)}{\partial x^2} (x - x_{t})^2
\]

Substituting Eq.(7) into Eq.(1) under boundary conditions (2)-(5) leads to a general differential equation of the surface potential distribution \( \phi_{2j}(x, y) \) in the region-2 as

\[
\frac{\partial ^2 \phi_{2j}(x, y)}{\partial x^2} + \frac{\partial ^2 \phi_{2j}(x, y)}{\partial y^2} = 0
\]

where \( t = \frac{L_{top}}{\varepsilon D_{top}} + \frac{L_{top}}{2} \) is defined as the effective thickness, and

\[
\phi_{2j}(x, y) = \phi_{2j}(x_0, y_0) - \phi_{2j}(y_0)
\]

is defined as the characteristic potential of the region-2.

Solving Eq.(8) with the boundary condition (6) gives the surface potential \( \phi_{2j}(x, y) \) and electric field \( E_{2j}(x, y) \) of the region-2 as

\[
\phi_{2j}(x, y) = \phi_{2j}(x_0, y_0) - \phi_{2j}(y_0)
\]

(10)

\[
E_{2j}(x, y) = \frac{V_d - \phi_{2j}(y_0)}{\sinh((L_{2j} - L_{j})/t)}
\]

(11)

As mentioned above, the region-1 and region-3 can be regarded as the special cases of the region-2. The surface potential and electric field distributions in the region-1 and region-3 can be obtained easily just by substituting corresponding boundary conditions and doping profiles into Eq.(9)-(11), and hence the expressions of the surface potential and electric field along the whole drift region are given by

\[
\phi_{2j}(x, y) = \phi_{2j}(x_0, y_0) - \phi_{2j}(y_0)
\]

(12)

\[
E_{2j}(x, y) = \frac{V_d - \phi_{2j}(y_0)}{\sinh((L_{2j} - L_{j})/t)}
\]

(13)
where \( i = 1, 2, 3 \), \( L_0 = 0 \), \( L_5 = L_d \), \( V_0 = 0 \) and \( V_5 = V_d \). \( \phi_i \) is the characteristic potential of the region-i. For a Dual-CL SOI device, \( \phi_i = qN_{i}\phi_i \) is the voltage of the surface electric field distribution of silicon and the buried oxide layers are assumed as linear and \( \phi_i \) is obtained from Eq.(9).

Utilizing the continuity conditions of the lateral electric fields at the interfaces of region-1/ region-2 and region-2/region-3, \( V_i \) and \( V_5 \) can be obtained by solving the matrix equation below (14).

\[
\begin{align*}
\sum_{i=1}^{3} \frac{a_{i1}E_i}{q}\left[ \text{coth}\left( L_i - L_{i+1} \right)/t_i \right] - \frac{a_{i2}E_i}{q}\left[ \text{csch}\left( L_i - L_{i+1} \right)/t_i \right] \\
- \frac{a_{i3}E_i}{q}\left[ \text{coth}\left( L_i - L_{i+1} \right)/t_i \right] + \frac{a_{i4}E_i}{q}\left[ \text{csch}\left( L_i - L_{i+1} \right)/t_i \right] \\
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix}
= \\
\begin{bmatrix}
3 \sum_{i=1}^{3} \frac{a_{i1}E_i}{q}\left[ \text{coth}\left( L_i - L_{i+1} \right)/t_i \right] - \frac{a_{i2}E_i}{q}\left[ \text{csch}\left( L_i - L_{i+1} \right)/t_i \right] + \frac{a_{i3}E_i}{q}\left[ \text{coth}\left( L_i - L_{i+1} \right)/t_i \right] - \frac{a_{i4}E_i}{q}\left[ \text{csch}\left( L_i - L_{i+1} \right)/t_i \right]
\end{bmatrix}
\end{align*}
\]

Note that Eq.(12) and Eq.(13) with different simplified forms are available for the other SOI devices with one/two/three doping layers in the drift region, such as single RESURF structure \( N_{\text{top}} = P_{\text{top}} = 0 \) \[^{[13]}\] , double RESURF structure \( N_{\text{top}} = P_{\text{top}} = 0 \) \[^{[14]}\] and triple RESURF structure \( N_{\text{top}} = 0 \) \[^{[11]}\].

### III. CALCULATION OF THE BREAKDOWN VOLTAGE

As well known, there are two electric field peaks at the surfaces of the P-well/N-drift and N-drift/N-drain junctions for lateral high voltage LDMOS transistors. When one of the magnitudes of the two electric field peaks reaches the critical field of silicon \( E_c \), the lateral breakdown occurs\[^{[15]}\]. Substituting Eq.(13) of the surface electric field distribution into \( E(0,0) = E_c \), \( E(L_d, 0) = E_c \), the lateral breakdown voltages \( BV_{\text{top,PN}} \) and \( BV_{\text{top,NN}} \) can be obtained, respectively. In the vertical direction, the electric field distributions in the top silicon and the buried oxide layers are assumed as linear and constant profiles, respectively\[^{[16-18]}\]. Fig. 2 shows the vertical electric field distribution when the breakdown occurs in the interface of Si/SiO\(_2\) under the drain. Obviously, the vertical breakdown voltage \( BV_{\text{ver}} \) can be calculated by the area under the curve of the vertical electric field distribution.

By summarizing the expressions of the lateral and vertical breakdown voltages, we obtain a matrix equation as following \[^{[19]}\].

\[
\begin{align*}
\begin{bmatrix}
BV_{\text{top,NN}} \\
BV_{\text{top,PN}} \\
BV_{\text{ver}}
\end{bmatrix}
= \begin{bmatrix}
a_{11} & a_{12} & a_{13} & a_{14} \\
a_{21} & a_{22} & a_{23} & a_{24} \\
a_{31} & a_{32} & a_{33} & a_{34}
\end{bmatrix}
\begin{bmatrix}
N_{\text{top}} \\
P_{\text{top}} \\
N_{\text{int}}
\end{bmatrix}
\end{align*}
\]

where \( N_{\text{int}} = qE_c \), \( q \) is the intrinsic concentration determined by the SOI material. The coefficient matrix \( \begin{bmatrix} a_{ij} \end{bmatrix}_{3,4} \) can be calculated by the expressions shown in appendix. The 1\(^{st}\)-3\(^{rd}\) rows of the matrix determine the N-drift/N-drain junction breakdown voltage, the P-well/N-drift junction breakdown voltage and the vertical breakdown voltage, respectively. The \( 1^{st}\)-4\(^{th}\) columns of the matrix represent the influences of the N-top, P-top, N-drift and intrinsic concentrations on the breakdown voltages, respectively.

### IV. RESURF CRITERION

In the SOI lateral high voltage device with a long drift region length, the breakdown point locates in the interface of Si/SiO\(_2\) and the breakdown voltage is determined by the doping profile of the drift region and the thickness of the top silicon and buried oxide layers. When the length of the drift region decreases, the lateral breakdown occurs before the vertical breakdown. The lateral breakdown voltage is determined by the two electric field peaks at the N-drift/N-drain and P-well/N-drift junctions\[^{[9]}\]. For an optimized device, the two electric field peaks are equal to the critical field of silicon \( E_c \) simultaneously when the breakdown occurs\[^{[10]}\]. Substituting Eq.(13) into \( E(0,0) = E(L_d, 0) = E_c \), the optimal breakdown voltage \( BV \) is derived as following \[^{[1]}\].
\[ BV = 2\phi_h + (\phi_i - \phi_f) \begin{bmatrix} \cosh \left( \frac{L_1}{t} \right) - \cosh \left( \frac{L_2}{t} \right) + \\ \coth \left( \frac{L_2}{2} \right) \left[ \sinh \left( \frac{L_1}{t} \right) - \sinh \left( \frac{L_2}{t} \right) \right] \end{bmatrix} \] (19)

For high voltage devices, the length of the P-top layer is approximately equal to the drift region length, i.e. \( L_i \approx 0, L_o \approx L_d \). In this case, a rough estimate of \( BV \) is simplified as
\[ BV = 2\phi_h = 2E_t \tan(0.5L_d/t) \] (20)

For the long drift region, substituting Eq.(9) into Eq.(20) yields
\[ Q_{\text{ass}}x = Q_{\text{ass}}^* \left( \frac{t + L_1 - t_1}{2} \right) \right] = \frac{e_i E_v}{q} \approx 10^{12} \text{ cm}^{-2} \] (21)

where \( Q_{\text{ass}} = N_d t_1, Q_{\text{ass}}^* = N_{ap} t_1, \) and \( Q_{\text{ass}}^* (t_2 - t_1) \) are the impurity doses of the drift region, N-top and P-top layers, respectively. This equation gives a unified single, triple and Dual-CL RESURF criterion for optimizing the device parameters. It implies that the optimal “total” dose of impurities including the drift region doping, the N-layer doping and the P-top layer doping is fixed for given structural parameters. For triple RESURF devices, by ordering \( N_{op} = 0 \) and Eq.(21) reduces
\[ Q_{\text{ass}}x = Q_{\text{ass}}^* \left( \frac{t + L_1 - t_1}{2} \right) \right] = \frac{e_i E_v}{q} \approx 10^{12} \text{ cm}^{-2} \] (22)

For single RESURF devices, by substituting \( N_{op} = P_{op} = 0 \), Eq.(21) is simplified to
\[ Q_{\text{ass}}x = \frac{e_i E_v}{q} \approx 10^{12} \text{ cm}^{-2} \] (23)

V. VERIFICATIONS AND DISCUSSIONS

In order to verify the proposed model, Fig. 3 shows the analytical results of the surface potentials and electric fields for the single RESURF, triple RESURF and Dual-CL SOI devices, together with the numerical results by Medici. The three devices have the same geometric parameters and are biased on the same reverse voltages. A good agreement between the analytical and numerical results can be found in general except the places near the junctions. Those differences are due to the ignorance of the curvature and built-in potential of junctions in the present model, which have little effect on the breakdown characteristic analysis. It is shown in Fig. 3(a) that the maximum potential drop of single RESURF locates near the P-well/N-drift junction, while that of the triple RESURF locates near the N-drift/N-drain junction, indicating the lateral voltage of the single RESURF is mainly sustained by the P-well/N-drift junction, while that of the triple RESURF is mainly sustained by the N-drift/N-drain junction. The potential drop of the Dual-CL at the P-well/N-drift junction is almost equal to that at the N-drift/N-drain junction and thus the lateral voltage is shared by the two junctions. Furthermore, Fig. 3(b) shows that the incorporation of the P-top layer leads to a movement of the maximum electric field from the P-well/N-drift junction to the N-drift/N-drain junction in the triple RESURF and Dual-CL devices. In the Dual-CL device, the heavily doped N-top layer results in a more uniform surface electric field distribution than the single and triple RESURF devices.

Fig. 4 gives the surface electric field distributions of Dual-CL SOI devices with different doping concentrations and thicknesses of the P-top layer. The dots and curves are the numerical and analytical results, respectively. The numerical results are shown to support the analytical results in general except the places near \( x = L_i \). Those differences are due to the neglect of the forward-bias junction at \( x = L_i \) in the present model. As the figure illustrates, besides the surface electric field peaks at the left and right edges of the drift region, there is
another new peak which appears at \( x = L_2 \), this new peak strongly depends on the parameters of the P-top layer. When the doping concentration or thickness of the P-top layer increases, the surface electric field peaks increase at \( x = L_2 \), while decrease at \( x = L_0 \). The reason is that the P-top layer benefits the depletion of the drift region and thus influences the profile of the electric field. Therefore, the electric field can be optimized and the breakdown voltage can be maximized by using the appropriate concentration and thickness of the P-top layer.

![Fig. 4. Surface electric field distributions of Dual-CL SOI devices with different doping concentrations (a) and thicknesses (b) of the P-top layer.](image)

![Fig. 5. Surface electric field distributions of Dual-CL SOI devices with different doping concentrations (a) and thicknesses (b) of the N-top layer.](image)

Fig. 5 illustrates the surface electric field distributions of Dual-CL SOI devices with different doping concentrations and thicknesses of the N-top layer. The comparison between Fig. 4 and Fig. 5 shows that the N-top and P-top layers have contrary effects on the surface electric field distribution. With the increase of \( N_{top} \) or \( t_t \), the surface electric field peak rises near the P-well/N-drift junction while reduces near the N-drift/N'-drain junction. When \( N_{top} \) and \( t_t \) are optimized, the surface electric field peaks at the P-well/N-drift and N-drift/N'-drain junctions are equal to the critical field of silicon \( E_c \) at the same time and the maximum breakdown voltage appears.
breakdown voltages. The drift region concentration in comparison with the lateral breakdown voltage is insensitive to the variation of the absolute value of element $N_{\text{abs}}$ concentration on the lateral breakdown voltages of the device according to Eq.(21). For the single RESURF device without the $N$-drift/N-well layer in the drift region, the maximum electric field locates on the surface of the $N$-drift/N$^+$-drain junction, and the breakdown voltage is determined by $a_{11} - a_{14}$ in Eq.(15). As Fig. 6(b) illustrates the coefficient $a_{ij}$ is positive, which results in a linear increase of the breakdown voltage with the increase of the doping concentration in the drift region. When the drift region concentration continues to increase, the maximum electric field moves to the interface of the $Si/SiO_2$ under the drain. The breakdown voltage is determined by $a_{11} - a_{14}$ in Eq.(15). The coefficient $a_{33}$ is negative and approaches 0 as shown in Fig. 6(b). As a result, the vertical breakdown voltage slightly decreases when the drift doping concentration increases. When the doping concentration in the drift region is large enough, the breakdown voltage linearly decreases with the increase of the drift region concentration. The breakdown location moves to the surface again due to the peak electric field of the P-well/N-drift junction and the breakdown voltage is determined by $a_{31} - a_{34}$ in Eq.(15). As Fig. 6(b) illustrates the coefficient $a_{34}$ is negative. In addition, triple RESURF and Dual-CL can lead to a drastically increase in the optimal drift region concentration, while a little change in the breakdown characteristics. It helps to optimize the tradeoff relationship between the breakdown voltage and the specific on-resistance.

Fig. 8 illustrates the dependence of the impurity doses of the N-top layer, the P-top layer and the drift region in an optimized device according to Eq.(21). For the single RESURF device without the N-top and P-top layers, the optimal drift region dose is almost equal to $1 \times 10^{15} \text{cm}^{-2}$ which is determined by both the thicknesses of the top silicon and buried oxide layers. The triple
RESURF device has a larger drift region impurity dose than the single RESURF device due to the incorporation of the P-top layer, resulting in a significant reduction of the specific on-state resistance. However, for the Dual-CL device with heavily doped N-top layer, the figure shows that the drift region dose is lower than the triple RESURF device to ensure the charge balance in the drift region. That means the specific on-state resistance of the drift region may be increased when the impurity dose of the N-top layer is high enough. So the structure parameters of the Dual-CL SOI device should be designed carefully to compromise the breakdown voltage and the specific on-state resistance.

VI. CONCLUSIONS

This paper focuses on the analytical model of SOI high voltage devices with Dual-CL structure. Firstly, the electrostatic potential and electric field distributions of single RESURF, triple RESURF and Dual-CL SOI high voltage devices are obtained by solving the 2-D Poisson’s equation in the drift region. Secondly, the lateral and vertical breakdown voltages are derived in the form of a matrix equation, considering the impacts of the N-top layer, P-top layer and the N-drift region. Thirdly, a unified RESURF criterion for optimizing the structure parameters of single RESURF, triple RESURF and Dual-CL SOI high voltage devices is proposed. According to the analytical model, the electric field reduction mechanism of the N-top and P-top layers is discussed. The dependence of breakdown voltage on the doping concentration in the drift region and the optimal relationship between the impurity doses of the N-top layer, P-top layer and the drift region are investigated. The proposed analytical model quantitatively explores the physical mechanism of the influences of the structure parameters on the breakdown voltage, and gives theoretically the reasons for the increase in the optimal drift doping concentration of the triple RESURF and Dual-CL SOI devices. Numerical simulations are performed to verify the analytical model and investigate the breakdown performance of the three devices. The numerical results are shown to support the analytical results. So the analytical model proposed here provides a useful design scheme and affords an effective way to improve the performance of Dual-CL SOI high voltage devices.

APPENDIX

The expressions for elements in matrix are given by

\[ a_{11} = \frac{1}{t_s} + \frac{t_s}{2} \left[ \cosh \left( \frac{L_d}{t} \right) - \cosh \left( \frac{L_u}{t} \right) \right] \]  
\[ a_{12} = \frac{t_s}{2} \left[ \cosh \left( \frac{L_d}{t} \right) - \cosh \left( \frac{L_u}{t} \right) \right] \]  
\[ a_{13} = 1 - \sech \left( \frac{L_d}{t} \right) \]  
\[ a_{14} = \tanh \left( \frac{L_d}{t} \right) \]  
\[ a_{21} = \frac{t_s}{t} + \frac{t_s}{2} \left[ \cosh \left( \frac{L_u}{t} \right) - \cosh \left( \frac{L_d}{t} \right) \right] \]  
\[ a_{22} = \frac{t_s}{2} \left[ \cosh \left( \frac{L_u}{t} \right) - \cosh \left( \frac{L_d}{t} \right) \right] \]  
\[ a_{23} = 1 - \cosh \left( \frac{L_d}{t} \right) \]  
\[ a_{24} = \sinh \left( \frac{L_d}{t} \right) \]  
\[ a_{31} = a_{32} = 0 \]  
\[ a_{33} = -\frac{1}{2} \left( \frac{t_s}{t} \right)^2 \]  
\[ a_{34} = \frac{t_s}{t} + \frac{t_s}{2} \left[ \cosh \left( \frac{L_u}{t} \right) - \cosh \left( \frac{L_d}{t} \right) \right] \]

where \( t_s \) is the depth of the drain junction.

ACKNOWLEDGMENT

The work is supported by the National Natural Science Foundation of China(60806027, 61076073), the Natural Science Foundation of Jiangsu Higher Education Institutions of China(08KJA510002, 09KJB510010), the Open Foundation of State Key Laboratory of Electronic Thin Films and Integrated Devices(KFJJ201011), the Research and Innovation Project for College Graduates of Jiangsu Province(CXZZ11_0382). The author is thankful to Dawei Zhong, Xueguan Wei, Jun Huang, Qin Xu, Jiafei Yao of Power and RF Microelectronic Lab for much valuable discussion and insight while they pursued this work.

REFERENCES


Tingting Hua was born in Yancheng, Jiangsu, China, in 1987. She received the B.S. degree from Nanjing University of Posts and Telecommunications, Nanjing, China, in 2009. She is currently studying for the Ph.D. degree in Nanjing University of Posts and Telecommunications. Her research interests in power device design and power device model.

Yufeng Guo received the Ph.D. degree in Microelectronics from University of Electronic Science and Technology of China, Chengdu, China, in 2005, B.S. and M.S. degrees in material engineering from Sichuan University, Chengdu, China, in 1996 and 2001, respectively. From July 1996 to September 1998, he was an assistant engineer in Luoyang Ship Material Research Institute. He joined Nanjing University of Posts and Telecommunications, Nanjing, China, in 2003 where he is currently a Professor and Vice-Dean at the College of Electronic Science & Engineering, Director, and Center of Electrical & Electronic Experiment Teaching. He is also a consultant of Semiconductor Device Laboratory, Asia University, Taichung, Taiwan. He is currently leading a research group in power semiconductor devices, power integrated circuits and RF integrated circuits. His current research interests include the characterization, simulation and modeling of power semiconductor devices, RF devices, and Nano CMOS devices. He has published over 50 papers in technical journals and refereed conferences in the above areas.


Ving Yu received the B.S. degree in Southeast University, Nanjing, China, in 1990, and the M.S. and Ph.D. degrees in Zhejiang University, Zhejiang, China, in 1993 and 1996, respectively. From 1996 to 2008, she worked in Fuzhou University. From 2001 to 2002, as a visiting scholar, she furthered her studies about RF MEMS switches at the National Research Council Institute for Microstructural Sciences (NRC-IMS), Canada. Since 2008, she joined Nanjing University of Posts and Telecommunications, Nanjing, China. She is currently a Professor at the College of Electronic Science & Engineering. Her current research interests include the simulation design, process fabrication and testing techniques of RF MEMS devices.

Xiaojuan Xia was born in jiangsu province,China.on January 23,1982. She received her bachelor's degree in electrical engineering in 2002 and her Ph.D.degree in 2009, from Southeast University, Nanjing, China. She now works in the College of Electronic Science and Engineering, Nanjing University of Posts and Telecommunications. She majors in analog integrated circuits and power integrated circuits.

Changchun Zhang received the B.S. and M.S. degrees in communication engineering in Guilin University of Electronic Technology (GUET), Guilin, China, in 2003, and 2006, respectively, and Ph.D. degree in electrical engineering in Southeast University, Nanjing, China, in 2010. Then he worked as a postdoc researcher in Ewha Womans University, Seoul, South Korea. Since December 2010, he joined Nanjing University of Posts and Telecommunications, Nanjing, China. His current research interests include IC designs on RFID transceivers and wireline transceivers.

Gene Sheu received the Ph.D. from University of Iowa and worked for RCA laboratory, Fairchild Semiconductor Corporation, director of NCR Micro-electronics, general manager of AT&T, etc. He is the Professor and Director of International Academic Exchange Program, Asia University. Taiwan. He is also the Asia University project leader of National nanotechnology development program, and Semiconductor team leader, Asia University Dept of Information Technology. His expertise is in the field of
A 200V Enhanced Dual Conduction Layer LDMOS with 12um

Drift Region

Jung-Ruey Tsai, Jia-Ming Guo, Shao-Ming Yang, Gene Sheu

Department of Computer Science and Information Engineering, ASIA University, Taichung,

Taiwan, Republic of China

Corresponding author:

Prof. Gene Sheu

Tel: +886-4-23323456#1784

Fax: +886-4-23325737

E-mail: g_shea@yahoo.com

Mailing address:

Department of Computer Science and Information Engineering, ASIA University,

1001 Ta-Hsueh Road, Hsinchu, Taiwan, 300, R.O.C.
A 200V Enhanced Dual Conduction Layer LDMOS with 12um Drift Region

Jung-Ruey Tsai, Jia-Ming Guo, Shao-Ming Yang, Gene Sheu

Department of Computer Science and Information Engineering, Asia University, Taichung, Taiwan, Republic of China

Abstract

A SOI LDMOS of 12 um drift region with enhanced dual conduction layers proposed in this paper has achieved 498 mohm mm\(^2\) on-state resistance, which is lower than any other state-of-art devices with structures including double RESURF, buried P-top, dual conduction layers, etc. The surface electrical potentials, electrical fields, breakdown voltages, and on-state resistances for devices with structures: single RESURF SOI LDMOS, buried P-top with dual conduction paths SOI LDMOS, and enhanced dual conduction layer SOI LDMOS are extensively analyzed by TSUPREM-4 and MEDICI simulations. The simulation results obtained show that a enhanced dual conduction layers SOI LDMOS device provides an on-state resistance reduction of 20% as compared with a buried P-top with dual conduction paths SOI LDMOS device and 10% as compared with a dual conduction layers SOI LDMOS device.

KEYWORDS: SOI, LDMOS, Dual conduction layers, Enhanced dual conduction layers, Breakdown voltage, On-state resistance.
1. Introduction

In recent years, the demand for power devices has increased dramatically, and especially the technology development in SOI (Silicon-On-Insulator) has attracted a lot of attention\(^1\). Devices made by SOI technology outperform the devices made by JI (junction isolation) due to their high speed performance, latch-up immunity, and superior isolation characteristics\(^2\). Therefore, the development of device focusing on SOI technology is an inevitable trend\(^3\).

Breakdown voltage and Ron (on-state resistance) are the most important device characteristics in LDMOS devices, but breakdown voltage and Ron have to be only traded off against each other. The challenge faced in this research is that the enhanced dual conduction layer LDMOS device is used to reduce the Ron without scarifying the breakdown voltage\(^4\).

The optimal breakdown voltage and Ron of a buried P-top LDMOS device as shown in Fig.1 (b). The drift region consists of an n-well diffusion in p-substrate. In the n-well the buried p-layer (called p-top) and the surfaced-layer (called n-top) are placed between the highly doped drain contact and the polysilicon gate. The p-top layer is connected to ground.
outside of the active area. The channel region is formed by lateral diffusion of a p-type implantation. The polysilicon gate length is 1.5 m and the channel length is measured to 0.3 m. The p- and n-top regions form a dual-layer RESURF of the drift region. The consequence is that depletion regions extending from both the substrate and the p-top region accomplish the depletion of the n-well. The pinch off voltage of the drift region is therefore lowered. This is used to increase the doping level of the n-well, without decreasing the breakdown voltage or causing punch through the narrow p-base region, thus decreasing the on-resistance. The n-top layer also provides an additional path for the current conduction in the on-state.

The optimal combination of breakdown voltage and Ron of a dual conduction layer LDMOS device as shown in Fig.1 (c) can be further improved by the buried P-top on which the enhanced N-doping is added; the buried P-top is used to compensate depleting the N-epi doping density increase in the drift region without increasing the electrical field; the enhanced N-doping on top of the P-top is used to reduce Ron down by 10\%\(^9\). The optimal combination of breakdown voltage and Ron of a dual conduction layer LDMOS device as shown in Fig.1 (d) can be further improved by extending the N-epi doping on the top of the buried P-top to the edge of the P-well; this extra extended N-epi can reduce Ron further by a further 20\%.

2. Simulation and Results

Fig.2 shows the breakdown voltages simulated by MEDICI\(^{10}\) for four different
LDMOS devices with various N-epi doping concentration in the drift region. The peak of the electric fields in the drift region will shift to the drain side as the doping concentration of N-epi decreases. Otherwise the peak of the electric fields in the drift region will shift to the gate side as the doping concentration of N-epi increases.

As shown in Fig. 2, the N-epi doping concentration to produce the best breakdown voltage for four different devices is located near to $5 \times 10^{15}$ cm$^{-3}$. However the breakdown voltage depending on N-epi doping concentration shows very little difference among LDMOS devices: buried P-top, dual conduction layer, and enhanced dual conduction layer.

Fig. 3 depicts the electric field distribution along the surface of four different LDMOS devices in the drift region. It is found that the electric field distribution for the buried P-top LDMOS devise is greater even when compared with those of the other three LDMOS devices known to have a better breakdown voltage.

Fig. 4 shows the Ron dependence on the N-epi doping concentration for four different LDMOS devices: (a) single RESURF, (b) buried P-top, (c) dual conduction layer, and (d) enhanced dual conduction layer. It is obvious that the higher the doping concentration in N-epi, the lower the on-state resistance. It is noted that the dual conduction layer LDMOS can reduce Ron to 10 % less than that achieved by the buried P-top LDMOS. The enhanced dual conduction layer LDMOS can further reduce Ron by a further 20 % compared with that achieved by the buried P-top LDMOS.
A single RESURF LDMOS achieves a high breakdown voltage by reducing N-epi doping concentration to make the drift region completely depleted, and therefore cause a very high Ron (on-state resistance). Ron can be improved in the buried P-top LDMOS by compensating depletion of the N-epi doping density increase in the drift region, but the improvement is still limited. Ron can be improved by 10% more on the dual conductance layer LDMOS device by adding the enhanced N-doping over the buried P-top layer. Ron can be further improved by 20% more on the enhanced dual conductance layer LDMOS device by extending the N-epi doping on the top of the buried P-top to the edge of the P-well. Fig. 5 shows that the safe operation area (SOA) of the enhanced dual conductance LDMOS device is better than those achieved by the other three LDMOS devices.

3. Conclusion

The enhanced dual conductance LDMOS device proposed in this paper has been thoroughly investigated in the areas of including electric potential, electric field, breakdown voltage, resistance dependence on the N-epi doping concentration, and etc.. The simulated results show that an enhanced dual conductance layer LDMOS device of a 12 μm drift region and 1.2 v threshold voltage which achieves more than 200 v on-state and off-state breakdown voltage, and 500 mohmm² on-state resistance, and the broad SOA(11), which can be applied to various high voltage power devices.
Reference


Figure Captions

Fig. 1: Schematic cross sections of SOI LDMOS device structures: (a) single RESURF; (b) buried P-top; (c) dual conduction layer and (d) enhanced dual conduction layer.

Fig. 2: (a) simulated Breakdown voltages as function of N-epi dose for different structures of LDMOS devices. (b) on-state resistances as function of N-epi dose for different structures of LDMOS devices.

Fig. 3: MEDICI simulations results to electric field distribution in the drift region along the surface of the different LDMOS structures.

Fig. 4: Safe operation area of SOI LDMOS devices for different structures applied gate voltage form 1V to 5V.
Table Captions

Table. 1
(a) 
Fig. 1
Fig. 1
Fig. 1
Fig. 1
Fig. 2
Fig. 2
Fig. 3
Fig. 4
Table 1.
Breakdown voltage (BVoff), on-state resistance (Ron), Baliga’s FOM (BFOM), for various structures. Data from this paper, conventional, Conventional, VLD, LT data from [ ], VD data from [ ].

<table>
<thead>
<tr>
<th>Structure (Ld=12um)</th>
<th>BVoff (V)</th>
<th>Ron (mΩmm²)</th>
<th>BFOM (kW/mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>249</td>
<td>833</td>
<td>297.6</td>
</tr>
<tr>
<td>Variation of Lateral Doping (VLD)</td>
<td>242</td>
<td>1131</td>
<td>206.8</td>
</tr>
<tr>
<td>Vertically Linear Doping (VD)</td>
<td>249</td>
<td>683</td>
<td>362.8</td>
</tr>
<tr>
<td>Linear Thickness (LT)</td>
<td>267</td>
<td>829</td>
<td>344</td>
</tr>
<tr>
<td>Enhanced dual conduction layer</td>
<td>210</td>
<td>498</td>
<td>354.2</td>
</tr>
</tbody>
</table>
專利申請證明文件(2 份)

美國發明專利申請

專利名稱：SEMICONDUCTOR STRUCTURE AND FABRICATION METHOD THEREOF

公司編號：98009

發明人：張義昭、杜尚暉、許健、張怡帆、白倪星

本案說明書圖式電子檔如附，敬請審閱並修改，並請於確認說明書內容無誤後，列印兩份表格並簽署英文姓名，並將簽署完成之表格正本傳回本部門。

請注意：表格日期請簽署西元年份如2009.1.1(勿簽民國年)，且兩份表格簽署日期請一致，或ASSIGNMENT簽署日期較DECLARATION晚，不可較早。


Walt, Wang 王威強
Legal Department
Vanguard International Semiconductor Corporation
Tel: 886-3-5770355 ext:2005
Fax:886-3-5773504
Email: wcwangd@vis.com.tw
美國發明專利申請

專利名稱：SEMICONDUCTOR STRUCTURE AND FABRICATION METHOD THEREOF

公司編號：98011

發明人：張義昭，杜尚輝，許健

Walt Wang 王威強
Legal Department
Vanguard International Semiconductor Corporation
Tel: 886-3-5770355 ext:2005
Fax: 886-3-5773504
Email: wcwangd@vis.com.tw

(See attached file: 0516-A42148-USd1.doc)

CONFIDENTIALITY NOTICE
The information contained in this email transmission, including all information attached to it, is confidential and privileged. If you are not the intended recipient, you are